

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Block Diagram	
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Voltage Rails

power plane	State	+B	+5VALW	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0		○	○	○	○	○	○ M3 Supported
S3		○	○	○	○	×	○ M3 Supported
S5 S4/AC		○	○	×	×	×	○ M3 Supported
S5 S4/ Battery only		×	×	×	×	×	
S5 S4/AC & Battery don't exist		×	×	×	×	×	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M1001_101xb	

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	✓	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	✓
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	✓	✓	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SMLOCLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	✓	X	✓	X	X	✓	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

USB Port Table

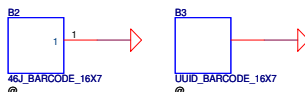
	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB 3.0 Port (Left Side)
		1	
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port
	UHCI2	4	Touch Panel
		5	
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	USB Port (Right Side)
	UHCI5	10	Mini Card(WLAN/BT)
		11	FPR
	UHCI6	12	Mini Card(WWAN)
		13	Camera

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
Nvidia	DIS@
PCH AUX Power	+3V_PCH@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N14M-GL	N14MGL@
GPU N14P-GV2	N14PGV2@
SIM Card Slot	3G@
Touch Panel	Touch@
Finger Print Board	FP@
SSD	SSD@

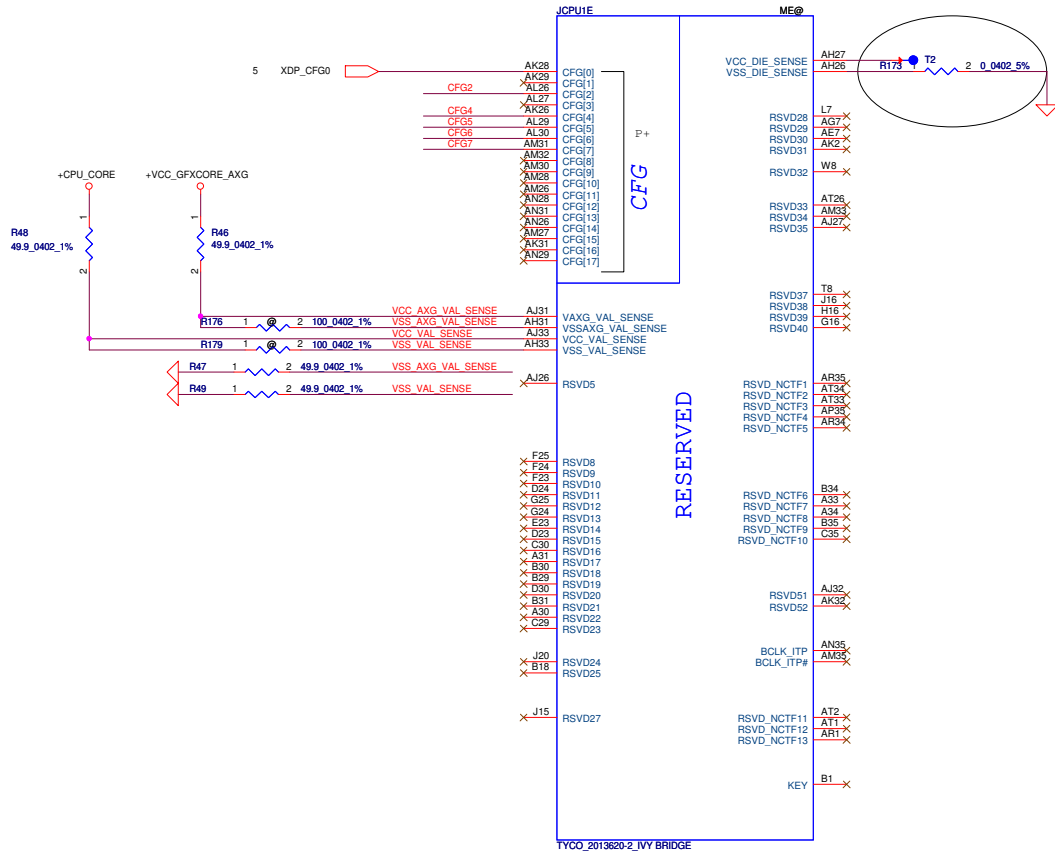
ZZZ5

 DA PCB
 DA8000TG00
 NM-A043

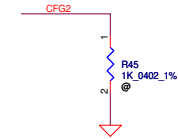


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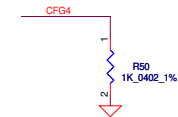


CFG Straps for Processor



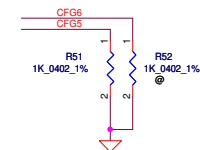
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>
------	---



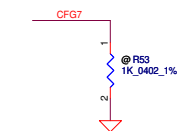
Display Port Presence Strap

CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
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PCIe Port Bifurcation Straps

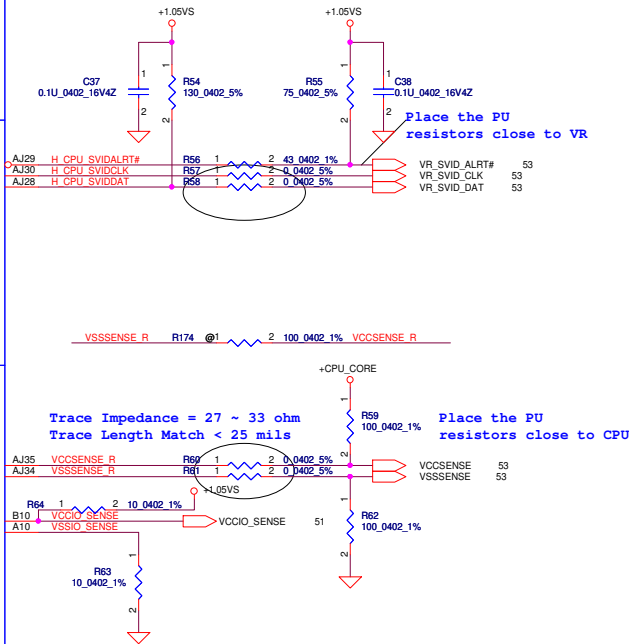
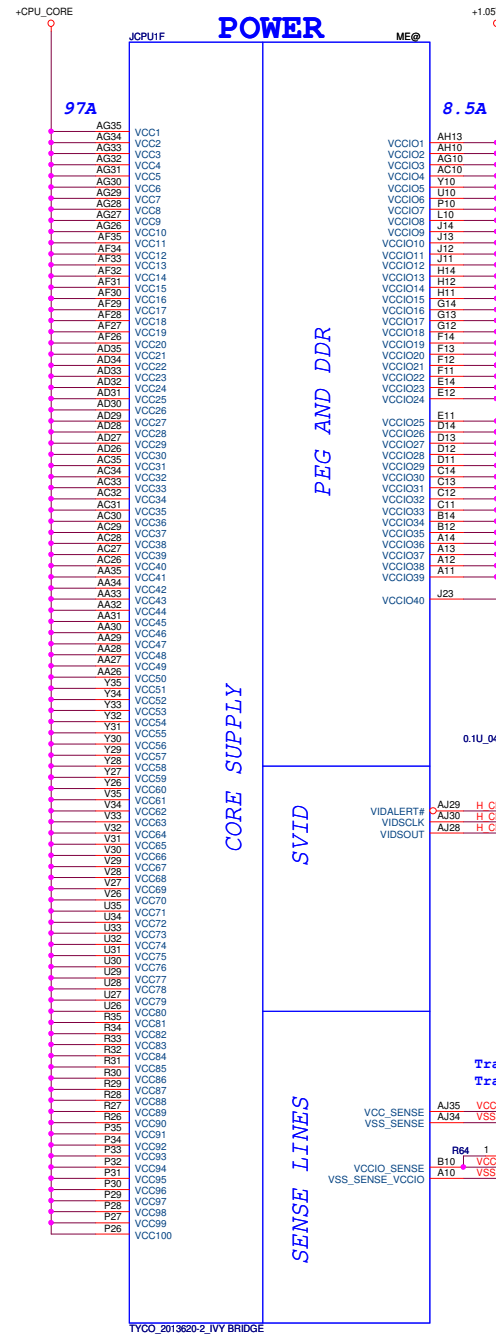
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>★ 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled; function 2 enabled)</p> <p>00: x8, x4, x4 - Device 1 functions 1 and 2 enabled</p>
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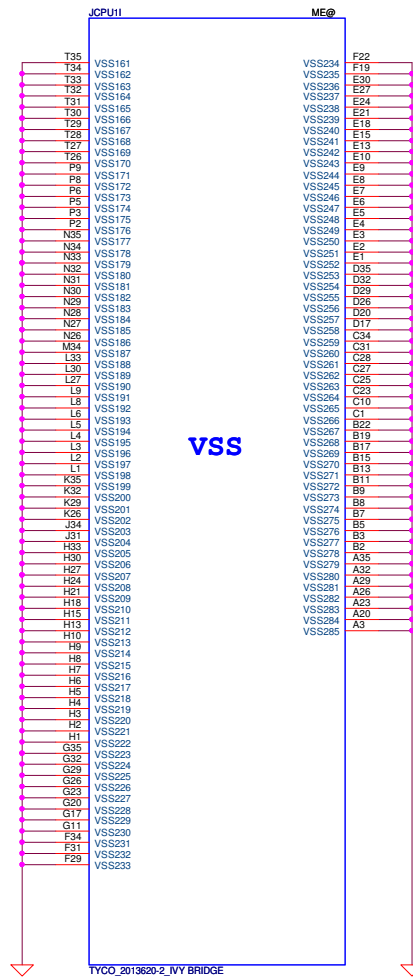
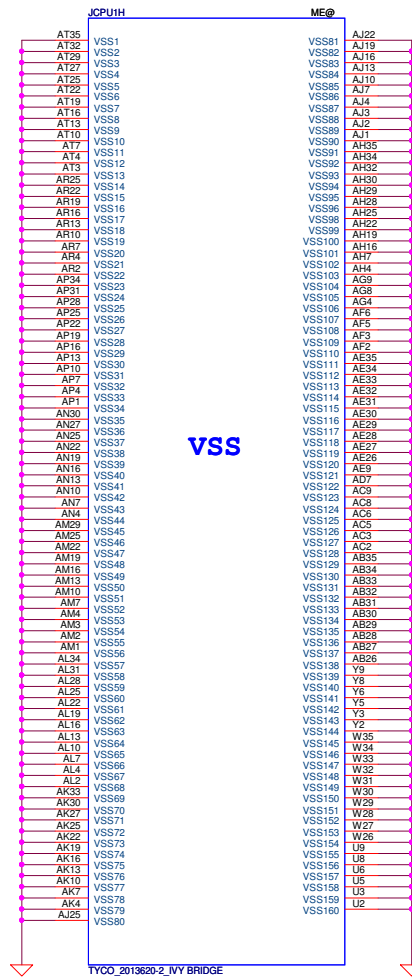
PEG DEFER TRAINING

CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
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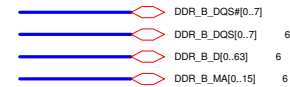
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PROCESSOR(5/7) PWR,BYPASS	
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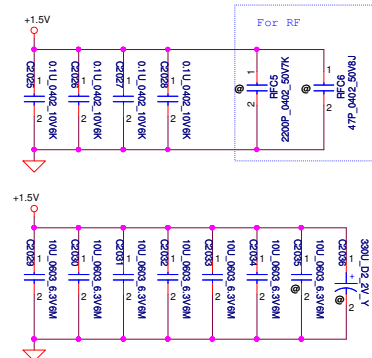
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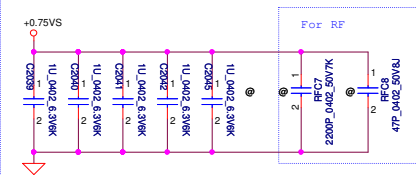
Rev
1.A




Layout Note:
Place near
JDIMM2

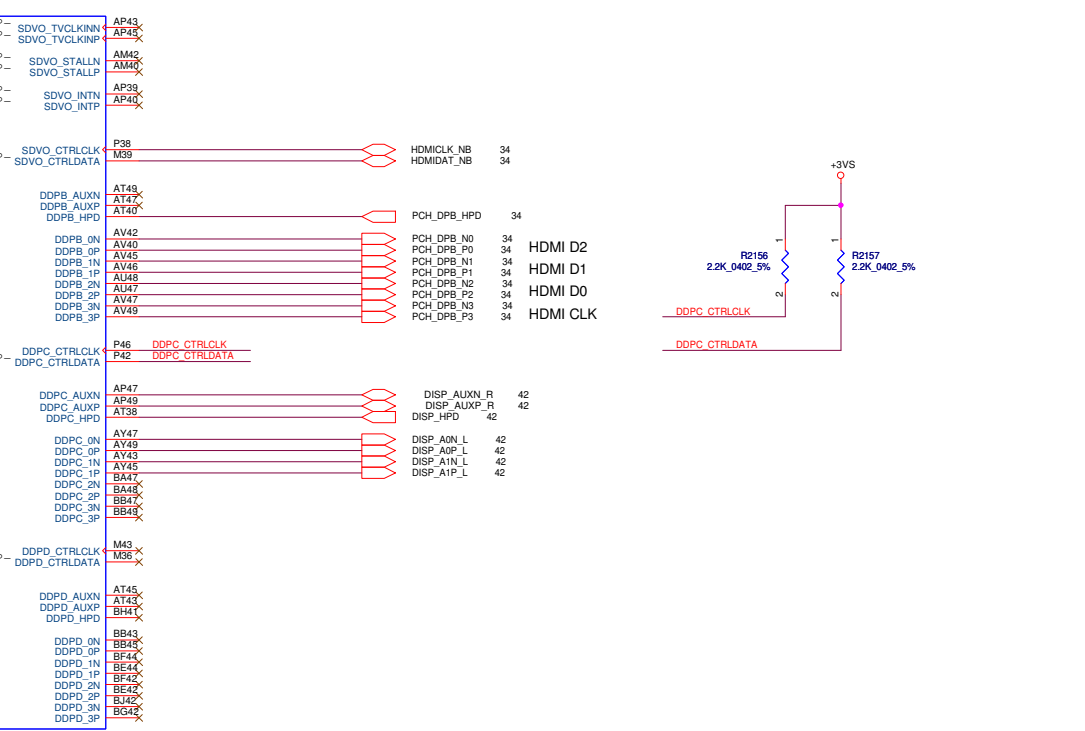


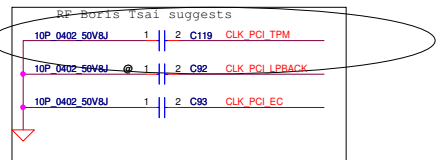
Layout Note:
Place near
JDIMM2.203, 204

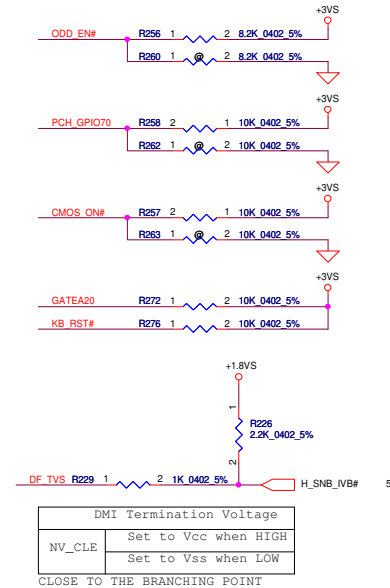
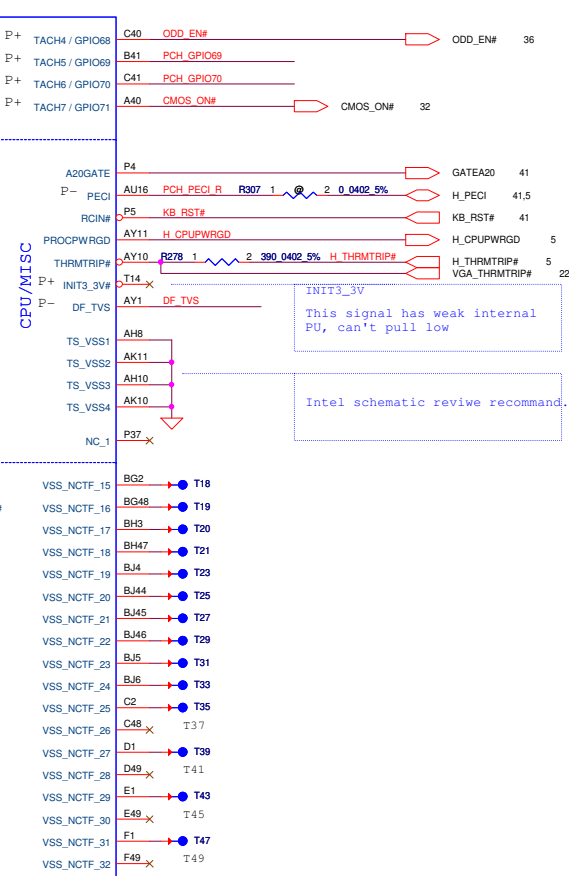
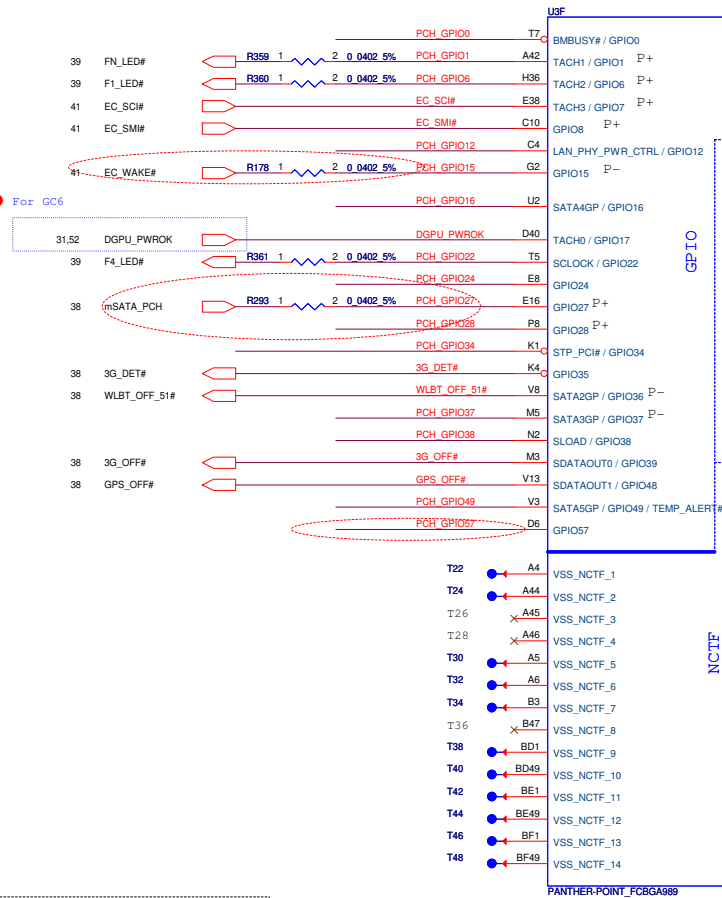
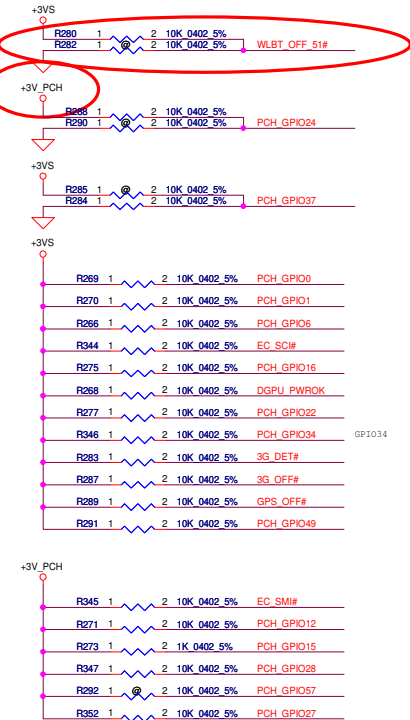


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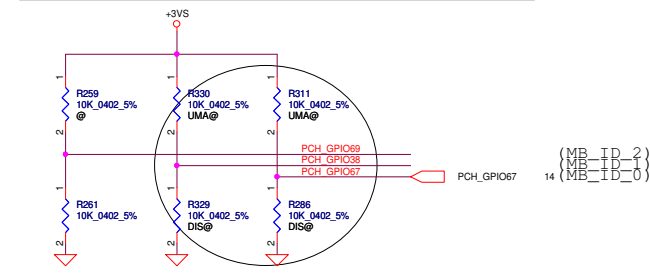


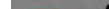






PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA



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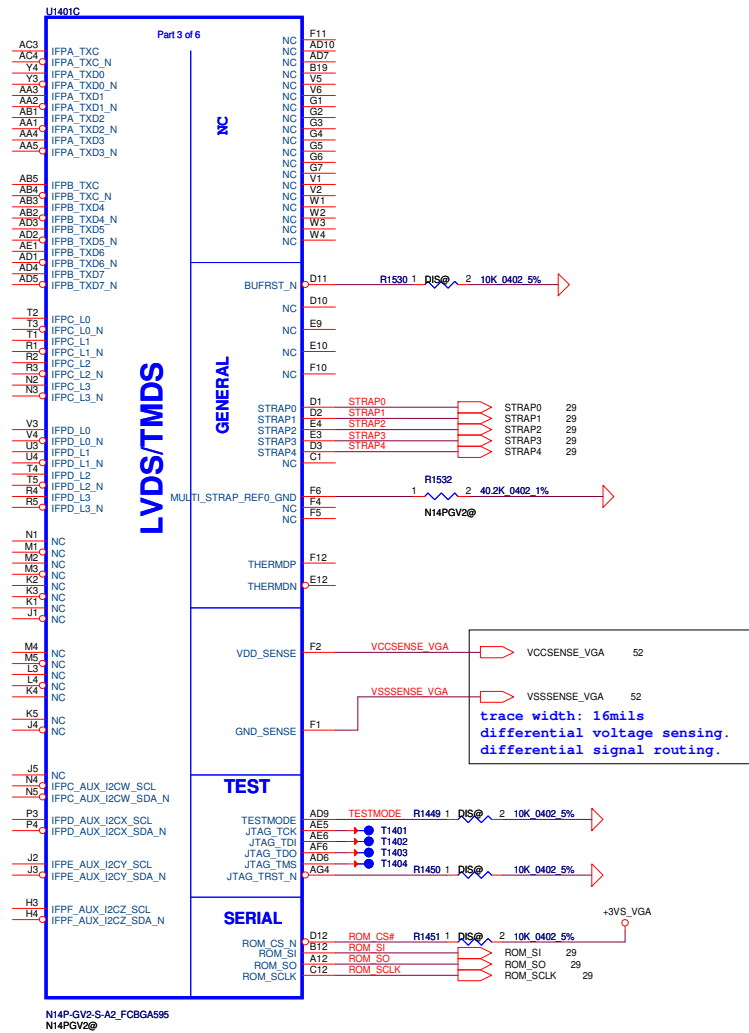
U3H			U3I		
H5	VSS[0]	AK38	AY4	VSS[159]	H46
AA17	VSS[1]	VSS[80]	AY42	VSS[159]	K18
AA2	VSS[11]	VSS[81]	AY46	VSS[160]	K26
AA3	VSS[3]	VSS[82]	AY8	VSS[162]	K39
AA33	VSS[3]	VSS[83]	B11	VSS[163]	K46
AA34	VSS[4]	VSS[84]	B15	VSS[163]	K7
AB11	VSS[5]	VSS[85]	B19	VSS[164]	L18
AB14	VSS[6]	VSS[86]	B21	VSS[165]	L2
AB39	VSS[7]	VSS[87]	B27	VSS[166]	L20
AB4	VSS[8]	VSS[88]	B31	VSS[167]	L26
AB43	VSS[9]	VSS[89]	B35	VSS[168]	L28
AB5	VSS[10]	VSS[90]	B39	VSS[169]	L36
AB7	VSS[11]	VSS[91]	B7	VSS[170]	L48
AC2	VSS[12]	VSS[92]	F45	VSS[171]	M12
AC19	VSS[13]	VSS[93]	BB12	VSS[172]	P16
AC21	VSS[14]	VSS[94]	BB16	VSS[173]	M18
AC24	VSS[15]	VSS[95]	BB20	VSS[174]	M22
AC33	VSS[16]	VSS[96]	BB22	VSS[175]	M24
AC34	VSS[17]	VSS[97]	BB24	VSS[176]	M30
AC48	VSS[18]	VSS[98]	BB28	VSS[177]	M32
AD10	VSS[19]	VSS[99]	BB30	VSS[178]	M34
AD11	VSS[20]	VSS[100]	BB36	VSS[179]	M38
AD12	VSS[21]	VSS[101]	BB4	VSS[180]	M4
AD13	VSS[22]	VSS[102]	BB46	VSS[181]	M42
AD19	VSS[23]	VSS[103]	BC14	VSS[182]	M46
AD24	VSS[24]	VSS[104]	BC18	VSS[183]	M8
AD26	VSS[25]	VSS[105]	BC2	VSS[184]	N18
AD27	VSS[26]	VSS[106]	BC28	VSS[185]	P30
AD33	VSS[27]	VSS[107]	BC26	VSS[186]	N47
AD34	VSS[28]	VSS[108]	BC32	VSS[187]	P11
AD36	VSS[29]	VSS[109]	BC36	VSS[188]	P18
AD37	VSS[30]	VSS[110]	BC40	VSS[189]	T33
AD38	VSS[31]	VSS[111]	BC42	VSS[190]	P40
AD39	VSS[32]	VSS[112]	BC46	VSS[191]	P43
AD4	VSS[33]	VSS[113]	BD36	VSS[192]	P47
AD40	VSS[34]	VSS[114]	BD46	VSS[193]	P7
AD42	VSS[35]	VSS[115]	BD5	VSS[194]	R2
AD43	VSS[36]	VSS[116]	BE2	VSS[195]	R48
AD45	VSS[37]	VSS[117]	BE40	VSS[196]	T12
AD46	VSS[38]	VSS[118]	BE4	VSS[197]	T31
AD8	VSS[39]	VSS[119]	BF10	VSS[198]	T37
AE2	VSS[40]	VSS[120]	BF12	VSS[199]	T4
AE3	VSS[41]	VSS[121]	BF16	VSS[200]	W34
AF10	VSS[42]	VSS[122]	BF20	VSS[201]	T46
AF12	VSS[43]	VSS[123]	BF22	VSS[202]	T47
AD14	VSS[44]	VSS[124]	BF24	VSS[203]	T8
AD16	VSS[45]	VSS[125]	BF26	VSS[204]	V11
AF16	VSS[46]	VSS[126]	BF28	VSS[205]	V17
AF19	VSS[47]	VSS[127]	BF30	VSS[206]	V26
AF24	VSS[48]	VSS[128]	BF36	VSS[207]	V27
AF26	VSS[49]	VSS[129]	BF38	VSS[208]	V29
AF27	VSS[50]	VSS[130]	BF40	VSS[209]	V31
AF29	VSS[51]	VSS[131]	BF8	VSS[210]	V36
AF31	VSS[52]	VSS[132]	BG17	VSS[211]	V39
AF38	VSS[53]	VSS[133]	BG21	VSS[212]	V43
AF4	VSS[54]	VSS[134]	BG33	VSS[213]	V7
AF42	VSS[55]	VSS[135]	BG44	VSS[214]	W17
AF46	VSS[56]	VSS[136]	BH11	VSS[215]	W19
AF5	VSS[57]	VSS[137]	BH15	VSS[216]	W2
AF7	VSS[58]	VSS[138]	BH17	VSS[217]	W27
AG19	VSS[59]	VSS[139]	BH19	VSS[218]	W48
AG2	VSS[60]	VSS[140]	H10	VSS[219]	Y12
AG31	VSS[61]	VSS[141]	H27	VSS[220]	Y38
AG38	VSS[62]	VSS[142]	H27	VSS[221]	Y4
AG48	VSS[63]	VSS[143]	H33	VSS[222]	Y42
AH11	VSS[64]	VSS[144]	H35	VSS[223]	Y46
AH3	VSS[65]	VSS[145]	H39	VSS[224]	Y8
AH36	VSS[66]	VSS[146]	H43	VSS[225]	BG29
AH39	VSS[67]	VSS[147]	H43	VSS[226]	N24
AH40	VSS[68]	VSS[148]	H43	VSS[227]	AJ3
AH42	VSS[69]	VSS[149]	D3	VSS[228]	AD47
AH46	VSS[70]	VSS[150]	D12	VSS[229]	B47
AH7	VSS[71]	VSS[151]	D16	VSS[230]	BE10
AJ19	VSS[72]	VSS[152]	D18	VSS[231]	BG41
AJ21	VSS[73]	VSS[153]	D22	VSS[232]	G14
AJ24	VSS[74]	VSS[154]	D24	VSS[233]	H16
AJ33	VSS[75]	VSS[155]	D26	VSS[234]	T36
AJ34	VSS[76]	VSS[156]	D30	VSS[235]	BG22
AK12	VSS[77]	VSS[157]	D32	VSS[236]	BG24
AK3	VSS[78]	VSS[158]	D34	VSS[237]	C22
			D38	VSS[238]	AP13
			D42	VSS[239]	M14
			D6	VSS[240]	AP3
			E18	VSS[241]	AP1
			E26	VSS[242]	BE16
			G18	VSS[243]	BC16
			G20	VSS[244]	BG28
			G26	VSS[245]	BJ28
			G28	VSS[246]	
			G36	VSS[247]	
			G48	VSS[248]	
			H12	VSS[249]	
			H18	VSS[250]	
			H22	VSS[251]	
			H24	VSS[252]	
			H26	VSS[253]	
			H30	VSS[254]	
			H32	VSS[255]	
			H34	VSS[256]	
			H36	VSS[257]	
			F3	VSS[258]	

PANTHER_POINT_FCBGA989

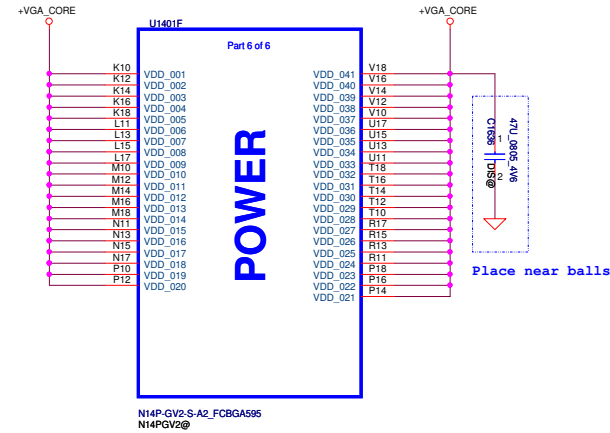
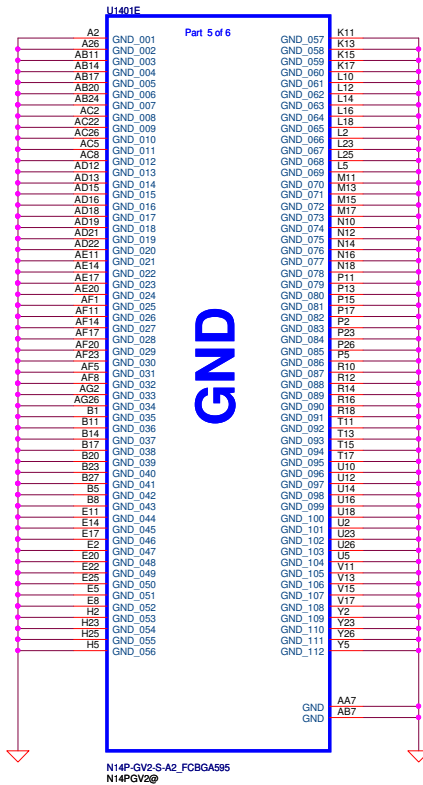
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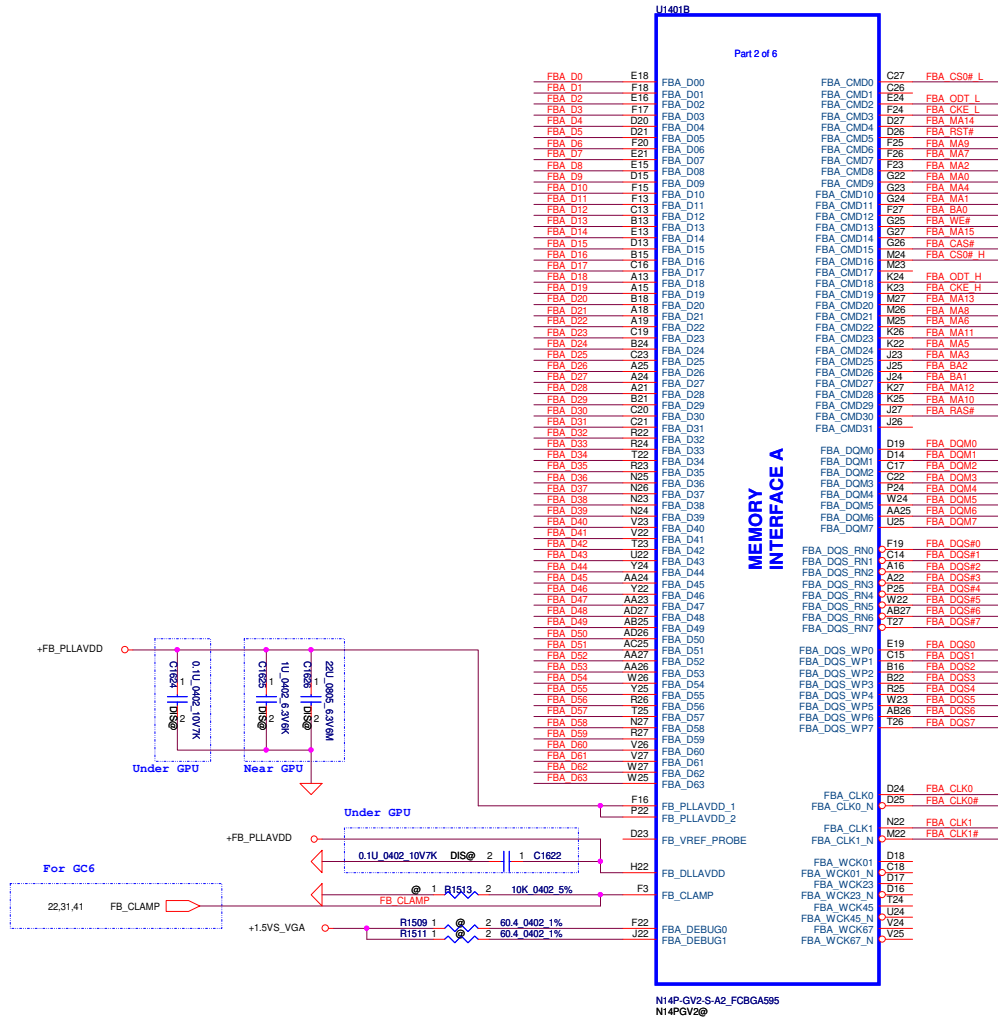


27,28 FBA_D[0..63] FBA_D[0..63]
27,28 FBA_DQM[7..0]
27,28 FBA_DQS[7..0]
27,28 FBA_DQS# [7..0]

FBA_MA[15..0] 27,28
FBA_BA[2..0] 27,28

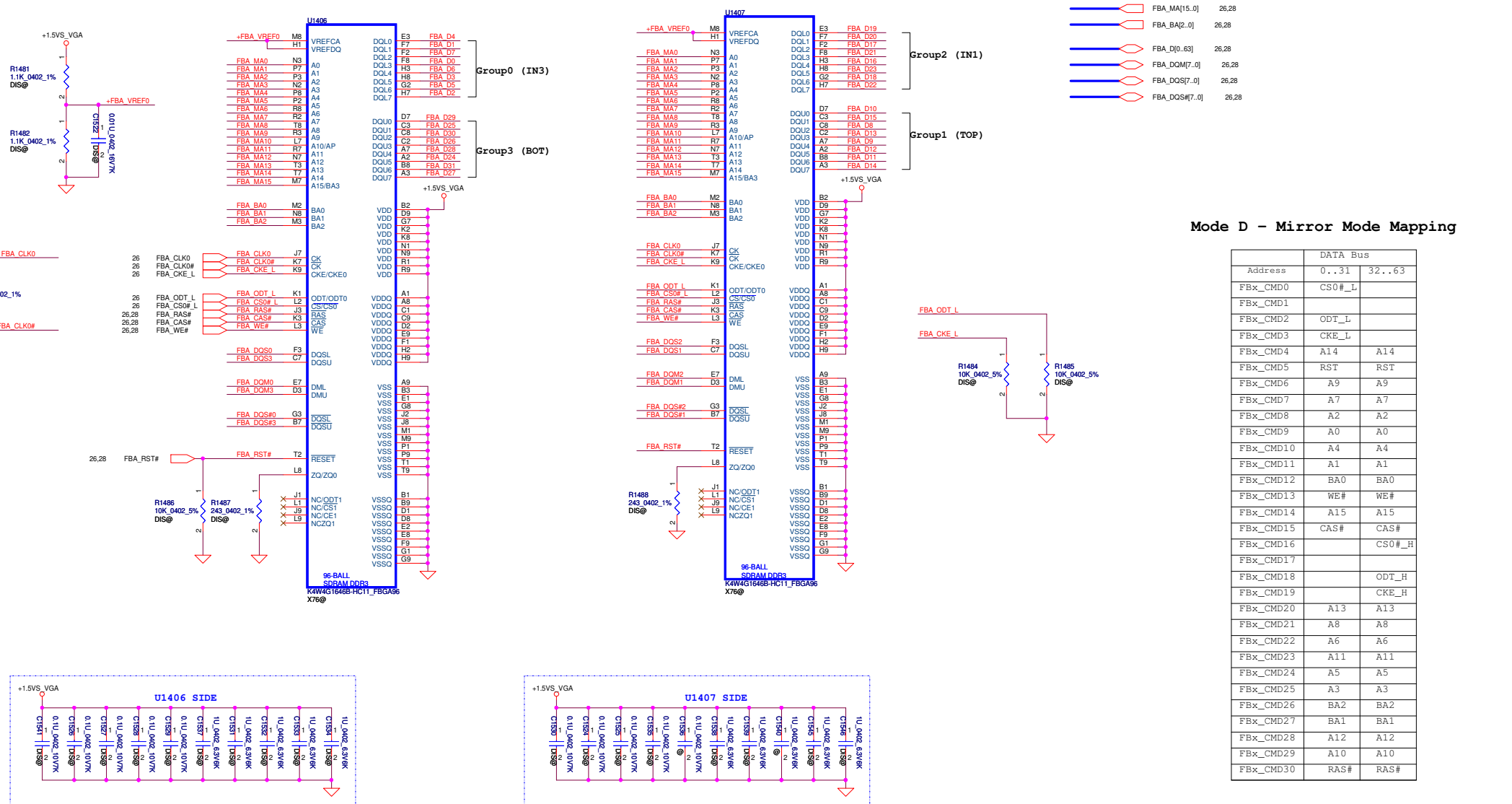
Mode D - Mirror Mode Mapping

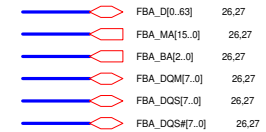
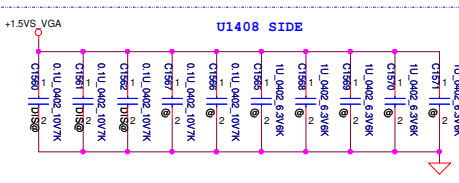
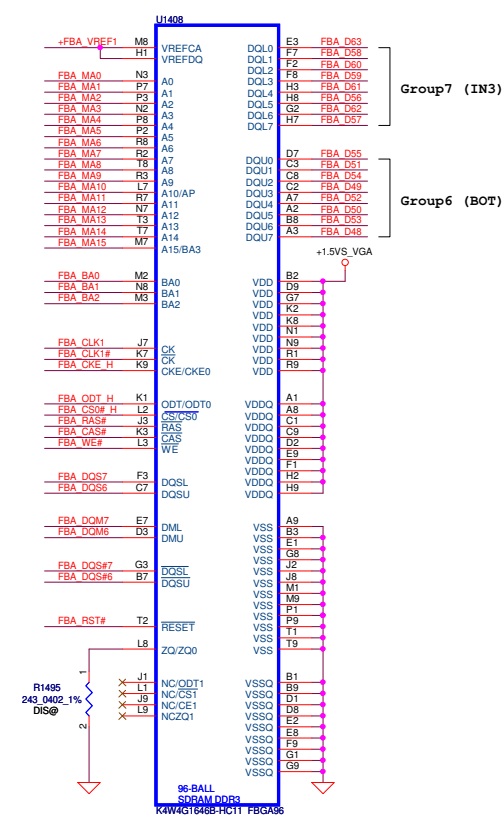
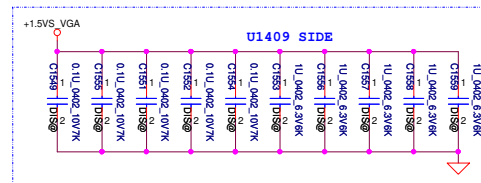
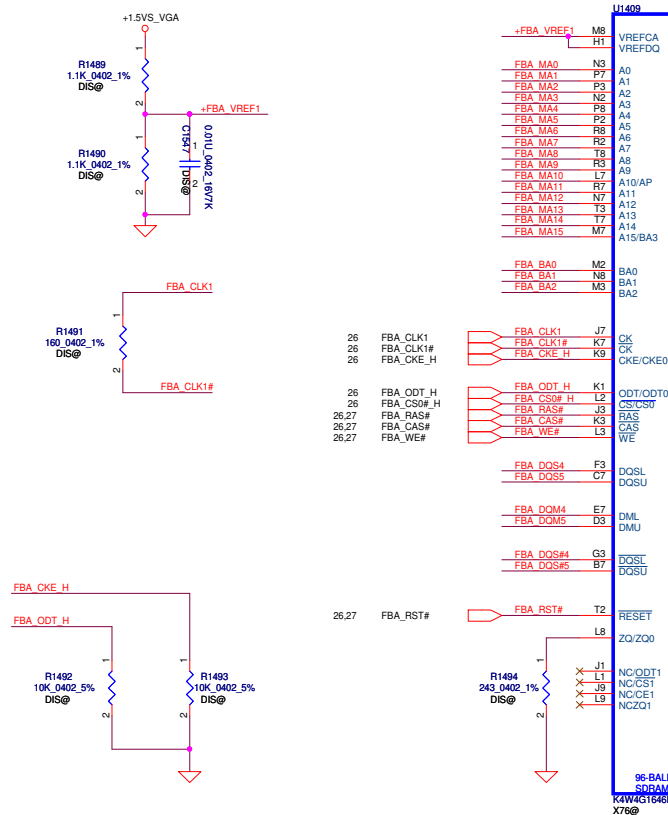
Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#_H	
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19	CKE_H	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



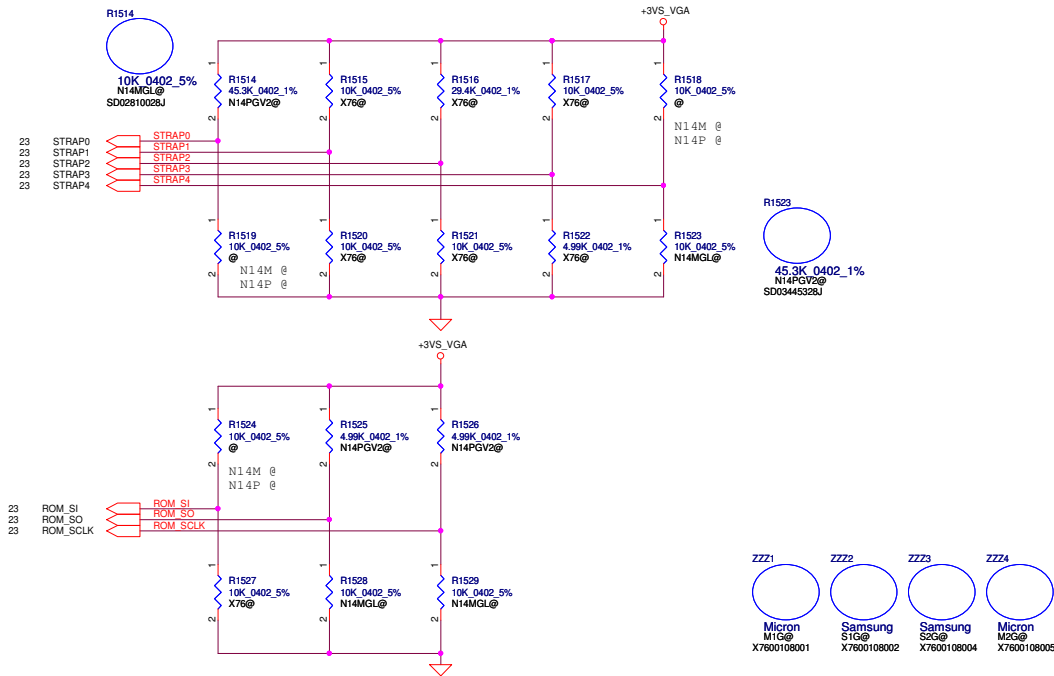
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	N14P_MEM Interface	
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Memory Partition A - Lower 32 bits



[illegible][illegible]

	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS0#_L	
FbX_CMD1		
FbX_CMD2	ODT_L	
FbX_CMD3	CKE_L	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE#	WE#
FbX_CMD14	A15	A15
FbX_CMD15	CAS#	CAS#
FbX_CMD16		CS0#_H
FbX_CMD17		
FbX_CMD18		ODT_H
FbX_CMD19		CKE_H
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS#	RAS#



GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A	PU 5K	PU 5K	PD 45K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		128Mx16								
	Micron 1000MHz	MT41J128M16JT-093G	PU 5K	PU 5K	PD 30K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		128Mx16								
	Samsung 900MHz	K4W4G1646B-HC11	PU 5K	PU 5K	PD 20K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		256Mx16								
	Micron 900MHz	MT41K256M16HA-107G	PU 5K	PU 5K	PD 10K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		256Mx16								

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14M-GL	Samsung 1000MHz	K4W2G1646E-BC1A	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K
		128Mx16								
	Hynix 1000MHz	H5TQ2G63DFR-N0C	PD 10K	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K
		128Mx16								
	Micron 1000MHz	MT41J128M16JT-093G	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K
		128Mx16								
	Samsung 900MHz	K4W4G1646B-HC11	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PU 10K	PD 10K
		256Mx16								
	Hynix 900MHz	H5TQ4G63MFR-11C	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K
		256Mx16								
	Micron 900MHz	MT41K256M16HA-107G	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PU 10K	PD 10K
		256Mx16								

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

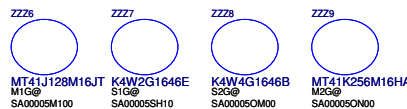
USER Straps	
User [3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

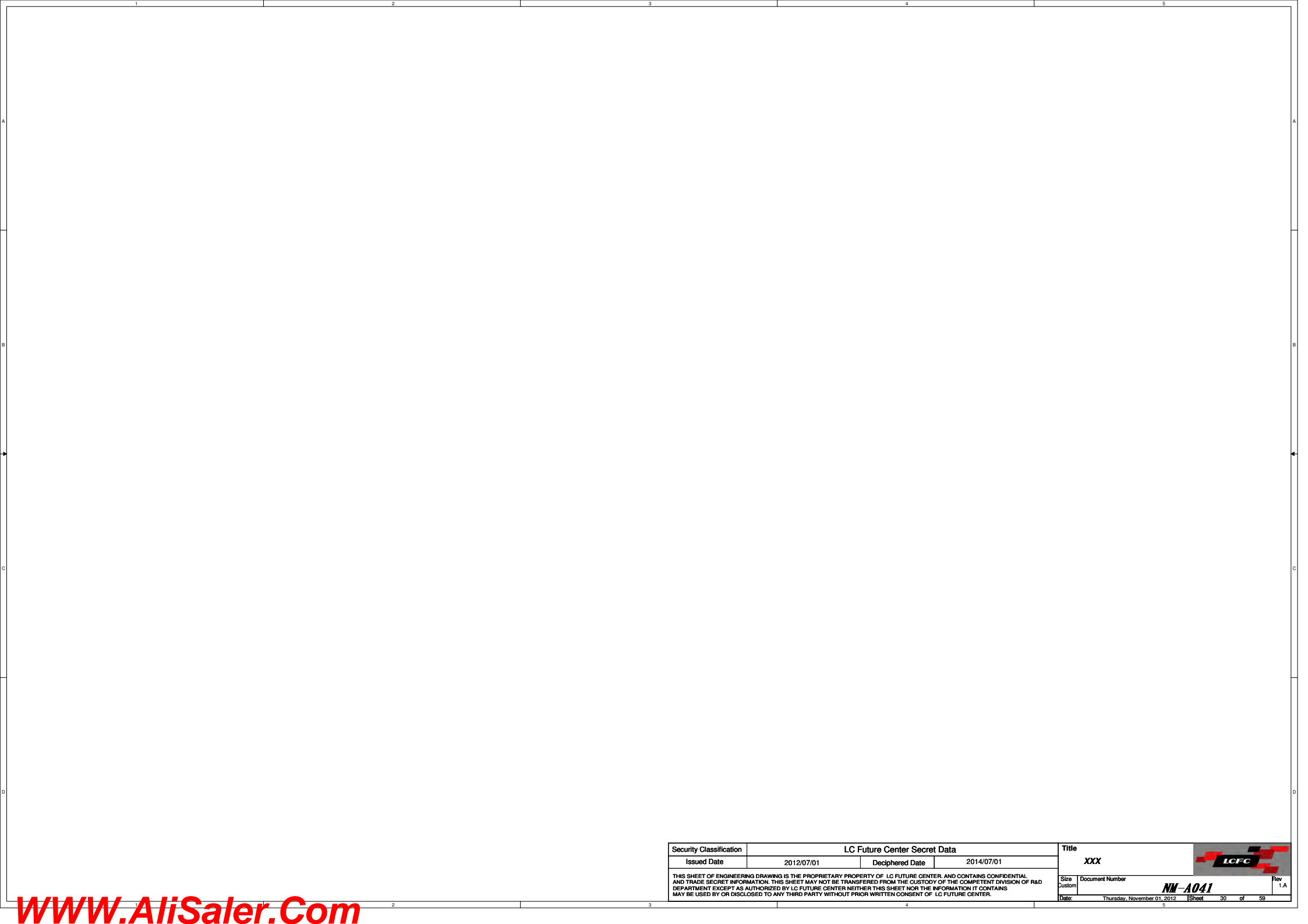
PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation


DP_PLL_VDD33V	
0	Reserved
1	Default

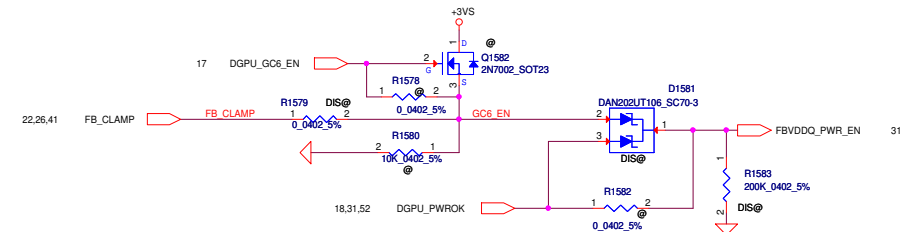
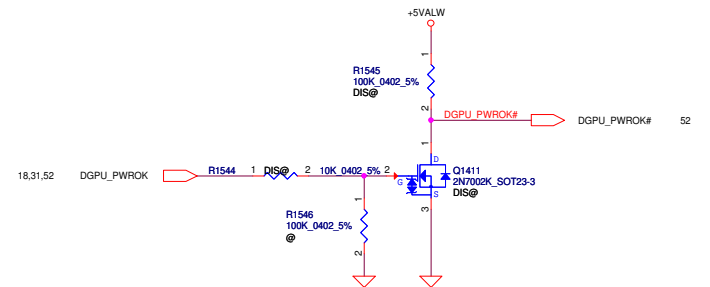
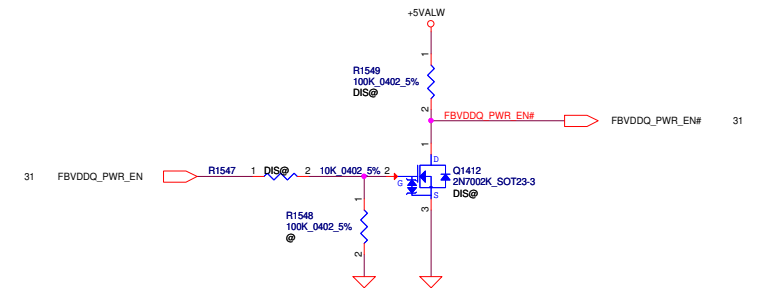


For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K

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Size Custom	Document Number			NW-A041	
Date:	Thursday, November 01, 2012		Sheet	29	of 59

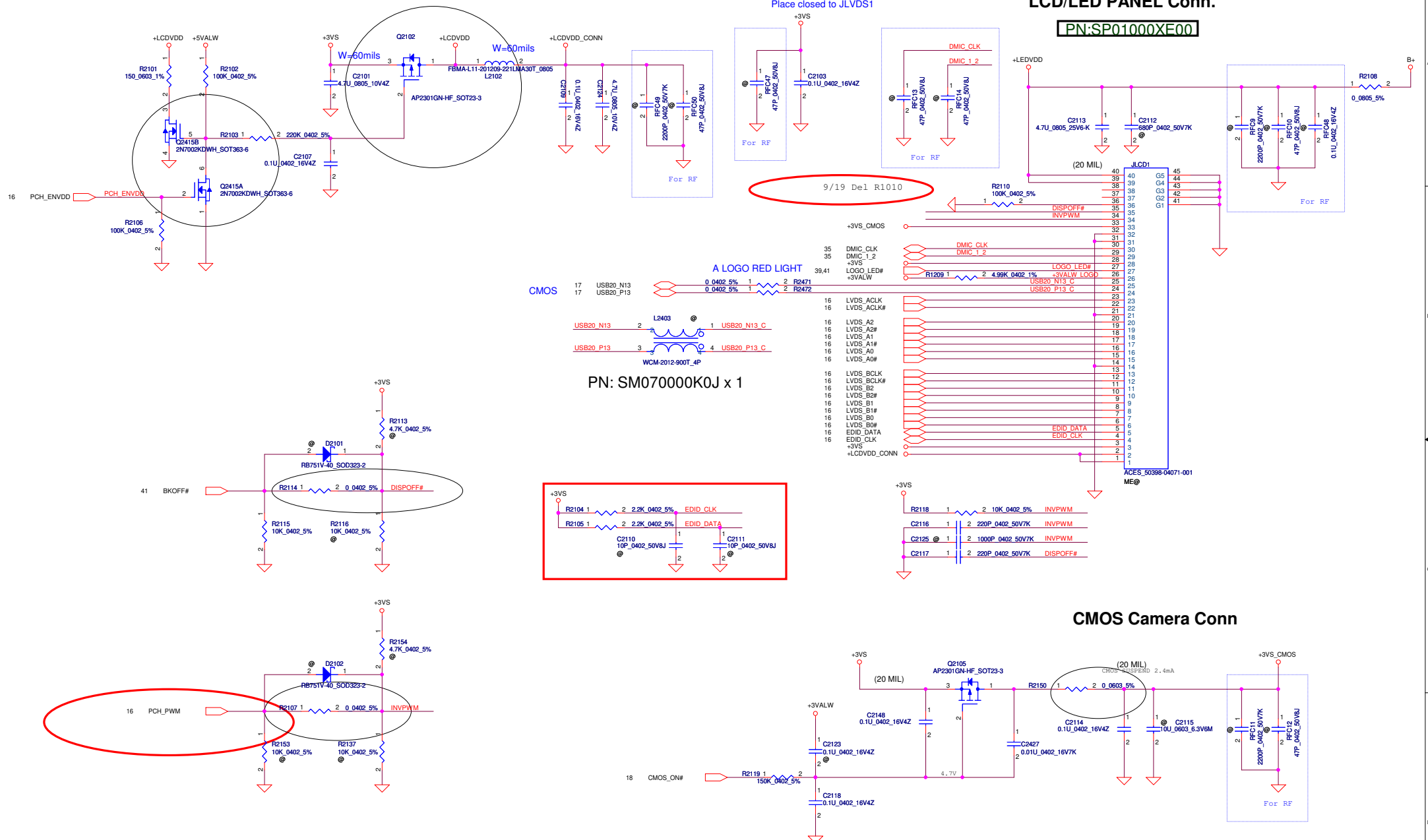


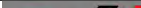
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Issued Date		2012/07/01		Deciphered Date			2014/07/01				
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Date:						Thursday, November 01, 2012				Sheet 30 of 59	

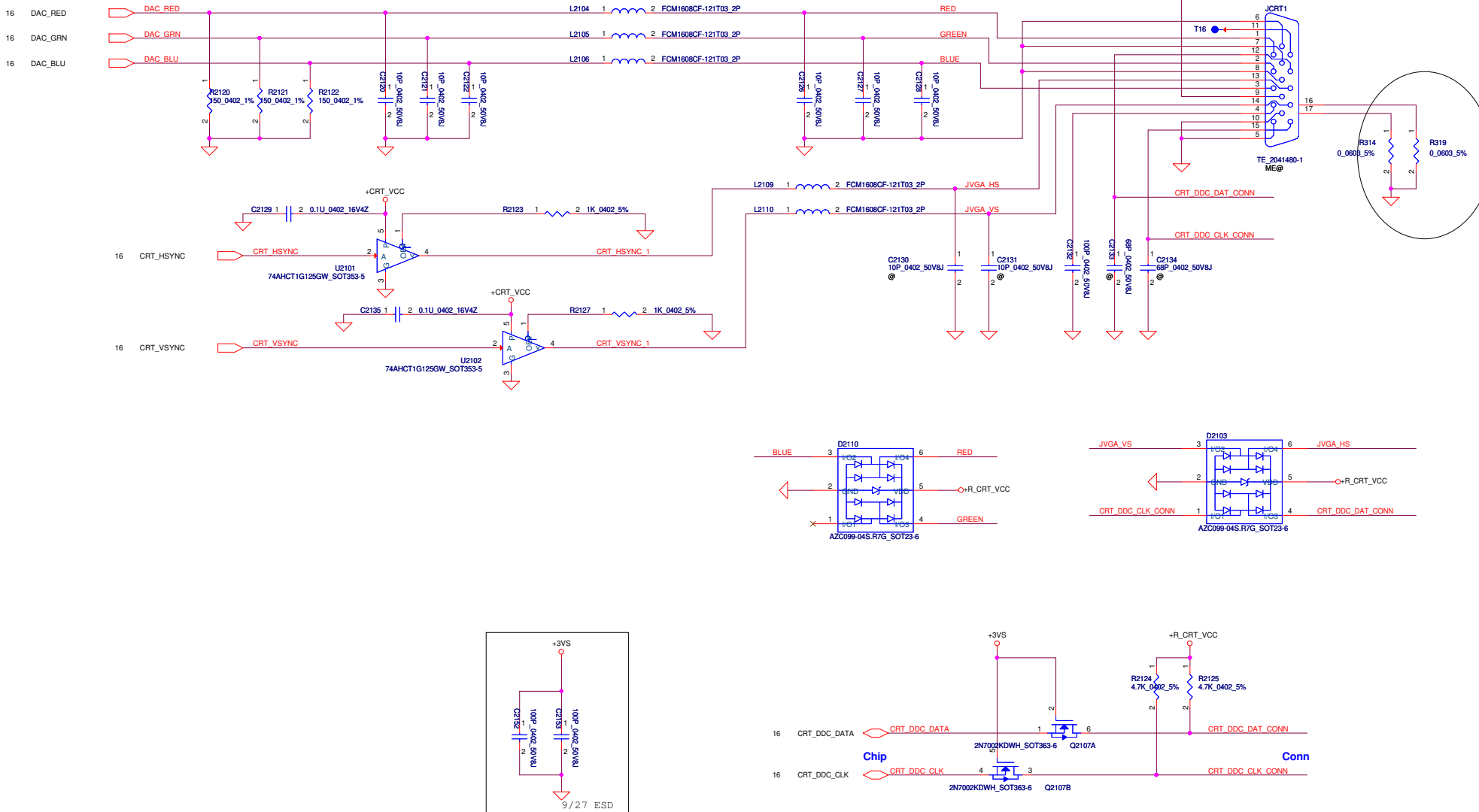



WWW.AliSaler.Com

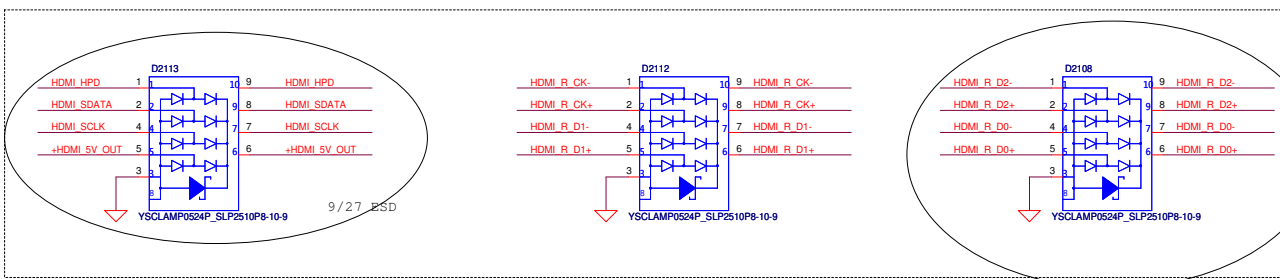
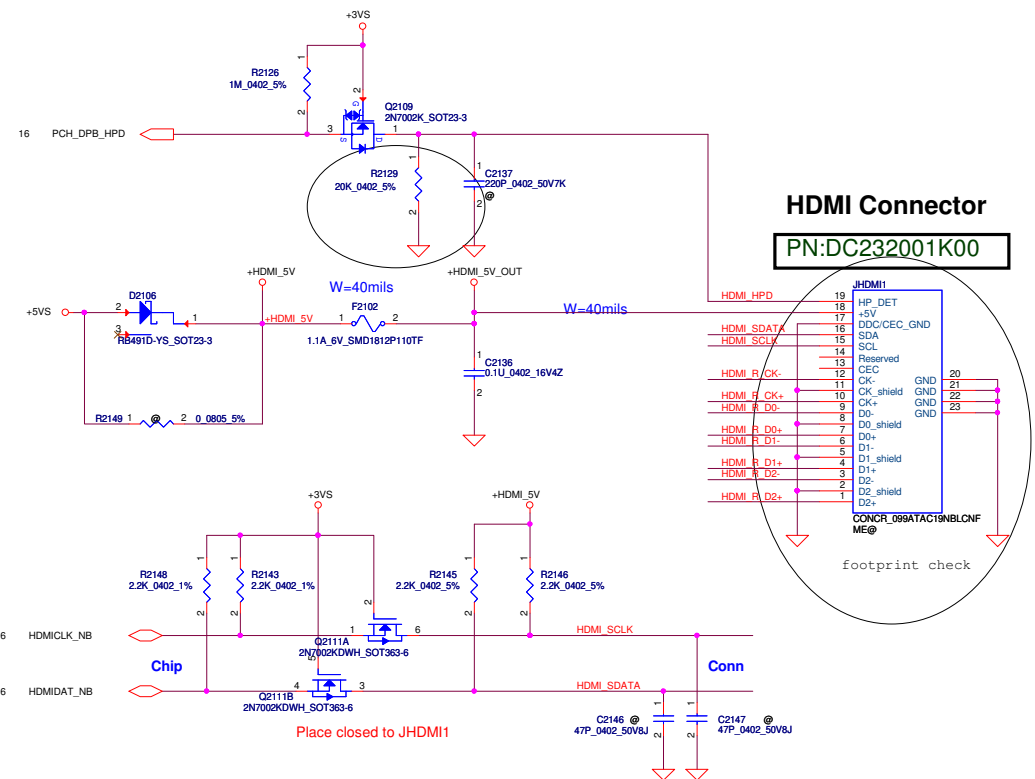
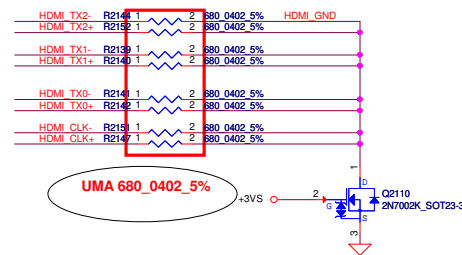
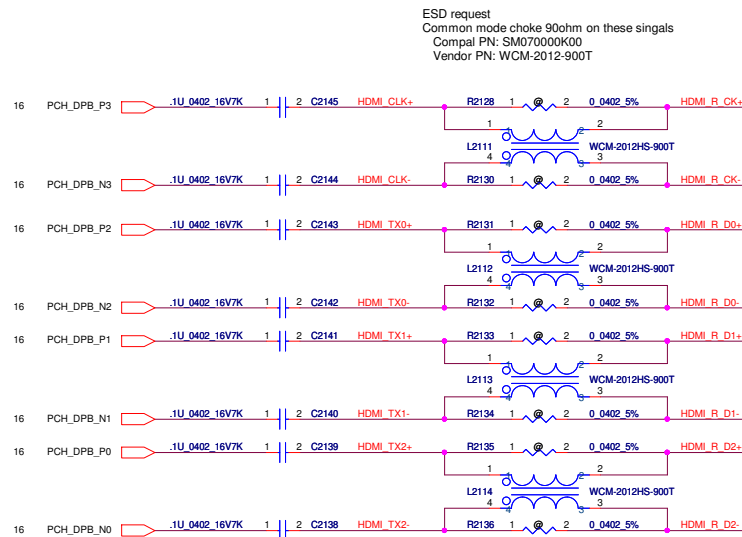
LCD POWER CIRCUIT




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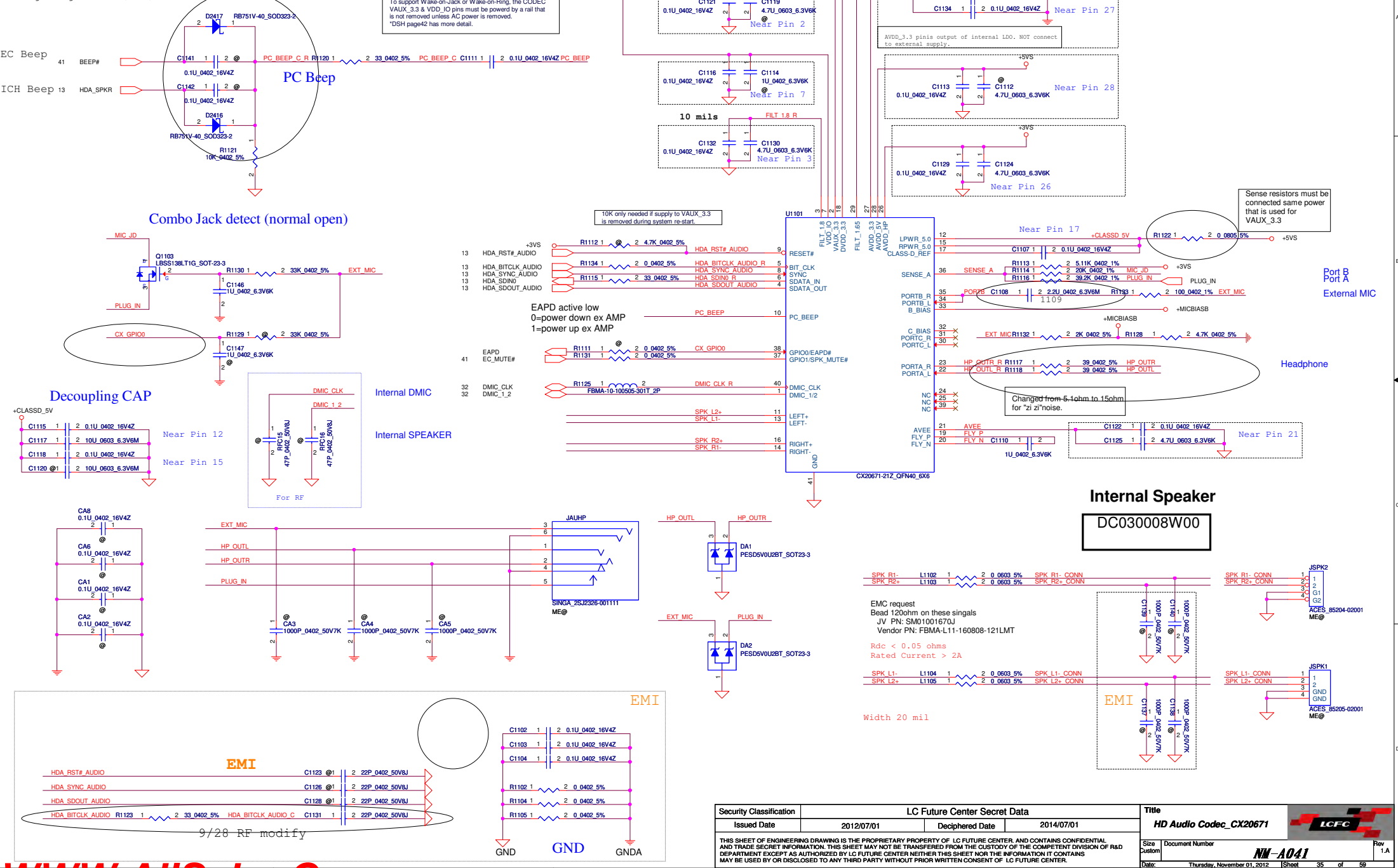


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						Custom	Document Number NW-A041
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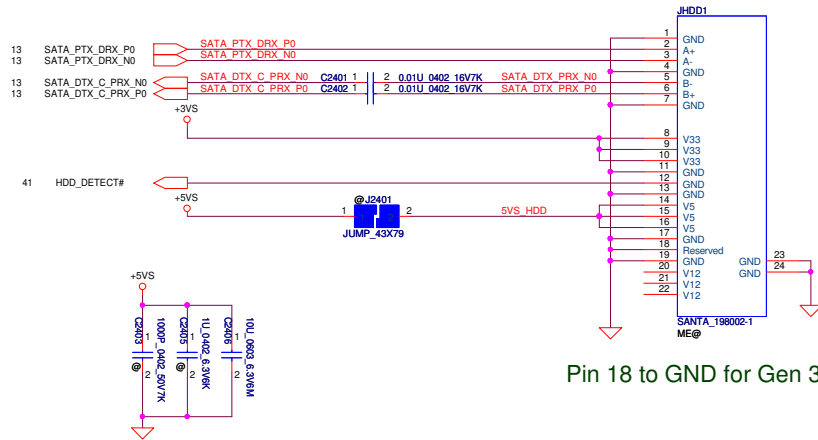
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Issued Date	2012/07/01	Deciphered Date	2014/07/01			
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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



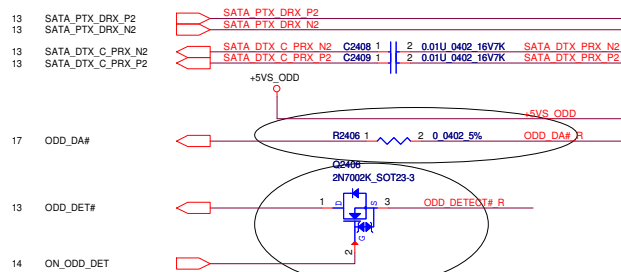
SATA HDD CONN.

PN:SP01001HE00

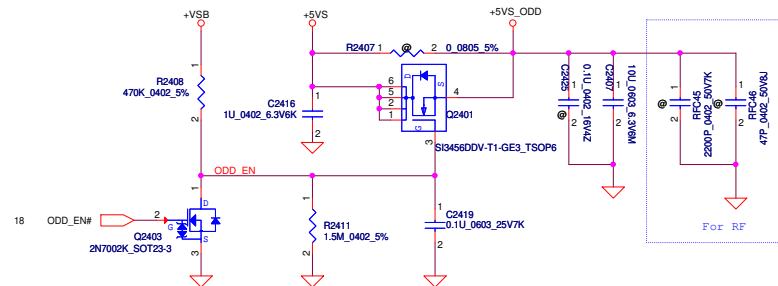
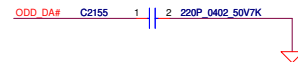
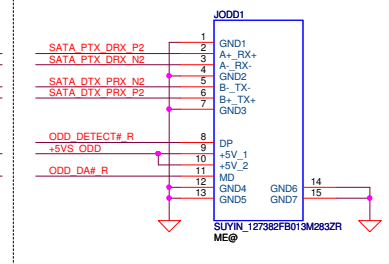


SATA ODD CONN.

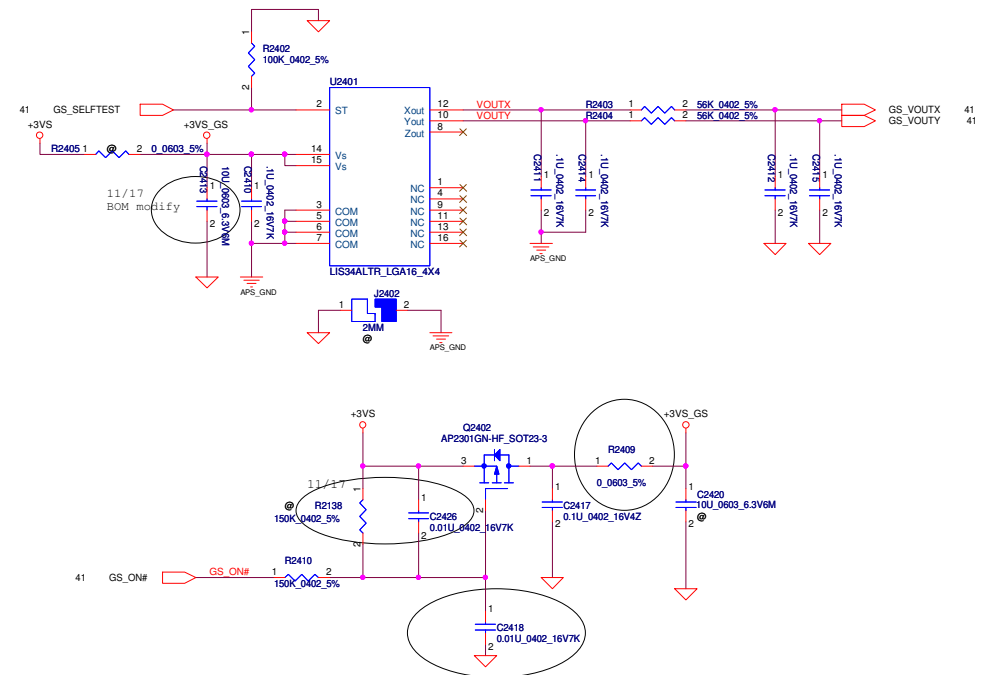
PN:SP01000TU10




for Edge 14''



APS G-Sensor



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Issued Date		2012/07/01		Deciphered Date	
2014/07/01		HDD/ODD/Card reader/G-Sen			
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Mini-Express Card(WLAN)

PN:SP07000JP00




Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

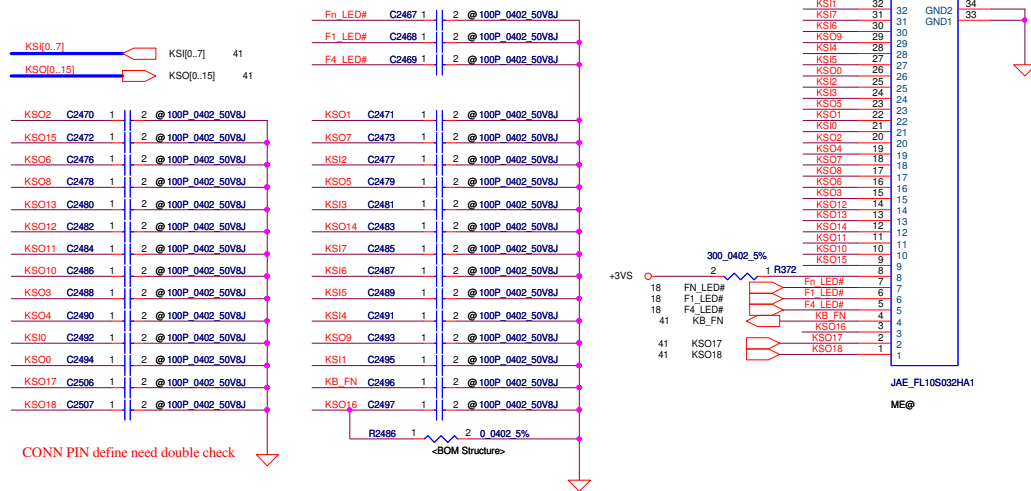
LPC FRAME# R	R2449 1	2	0.0402 5%	LPC FRAME#		LPC FRAME#	13,40,41
LPC AD3 R	R2455 1	2	0.0402 5%	LPC AD3		LPC AD3	13,40,41
LPC AD2 R	R2456 1	2	0.0402 5%	LPC AD2		LPC AD2	13,40,41
LPC AD1 R	R2457 1	2	0.0402 5%	LPC AD1		LPC AD1	13,40,41
LPC AD0 R	R2458 1	2	0.0402 5%	LPC AD0		LPC AD0	13,40,41
PLT RST# R	R2459 1	2	0.0402 5%	PLT RST#			
CLK PCI DB R	R2428 1	2	0.0402 5%	CLK PCI DB		CLK_PCI_DB	17,40

PN:SP01072413J

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Date:		Thursday, November 01, 2012		Sheet		38		of 50	

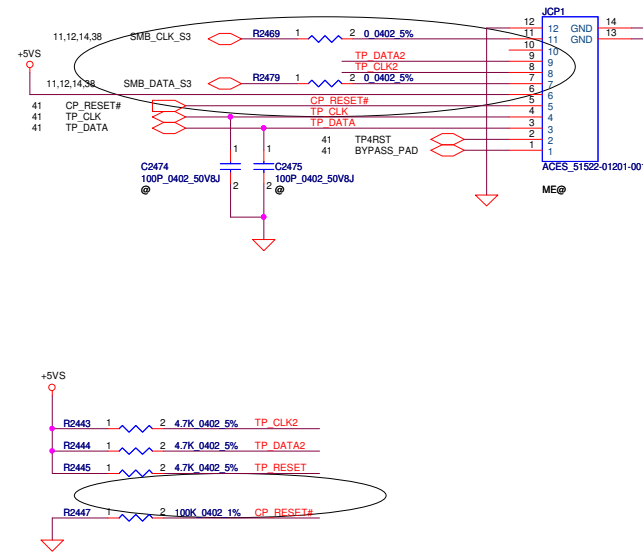
INT_KBD Conn.

PN:SP011208010



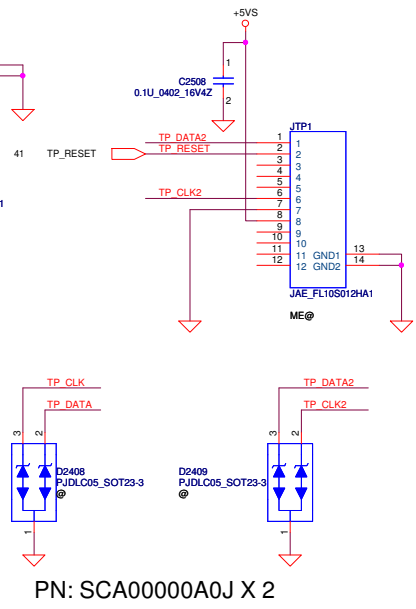
Click pad

PN:SP01001BX00

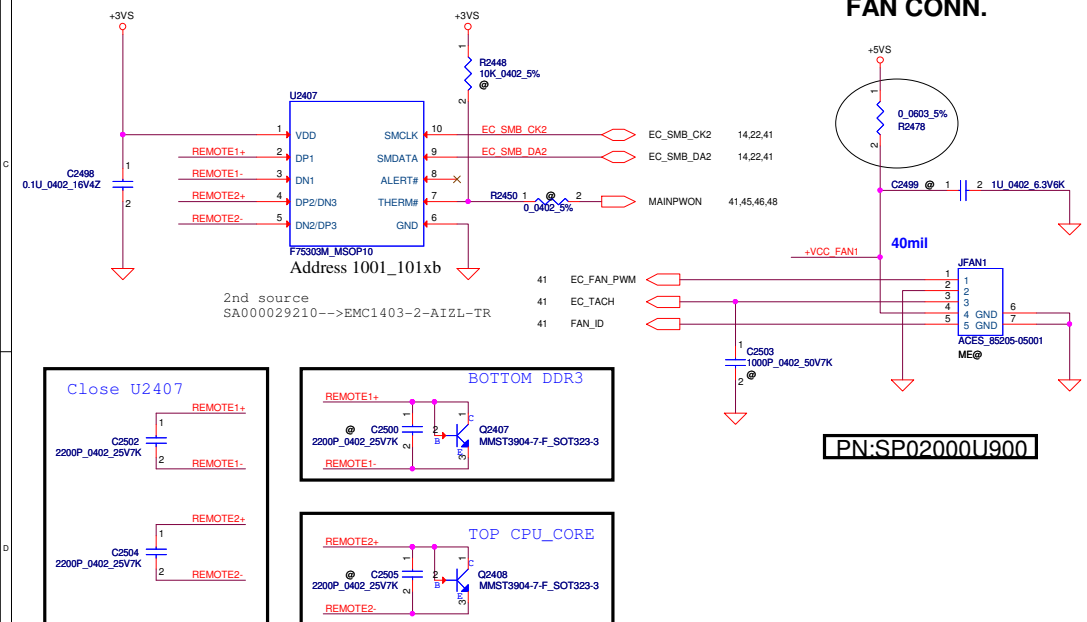


Track point

PN:SP01120802J

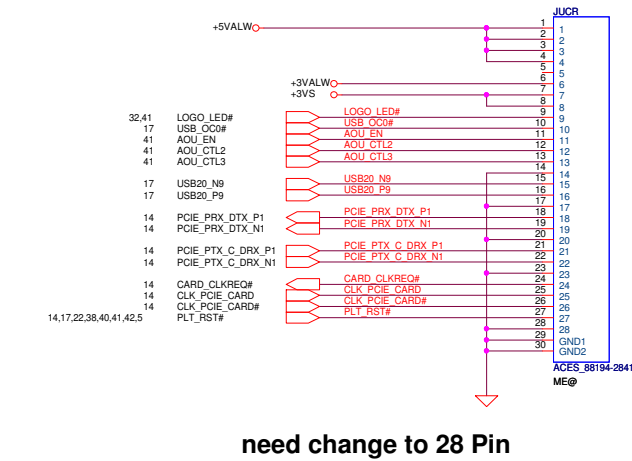



Fintek thermal sensor placed near by TOP DDR3



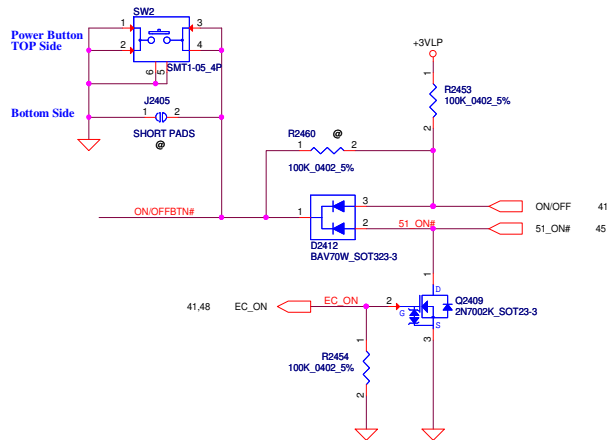
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Audio+CR Board

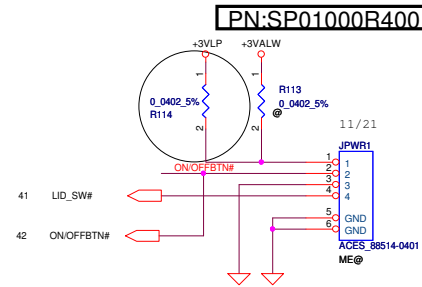


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				Custom	NW-A041	1.A	
Date:				Thursday, November 01, 2012	Sheet	39	of 59

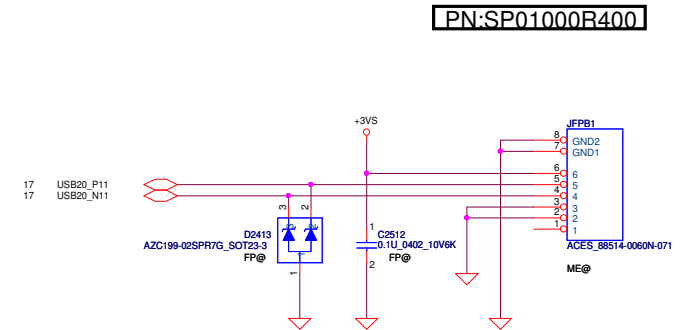
Power Button



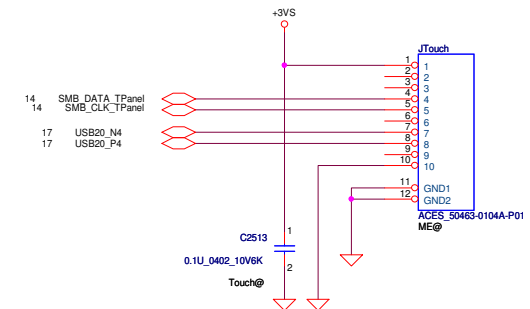
Power Button CONN.



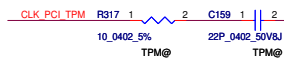
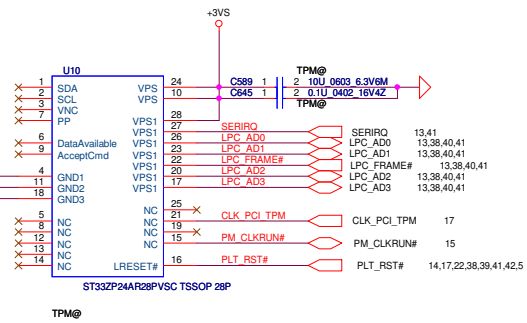
Finger Print Board



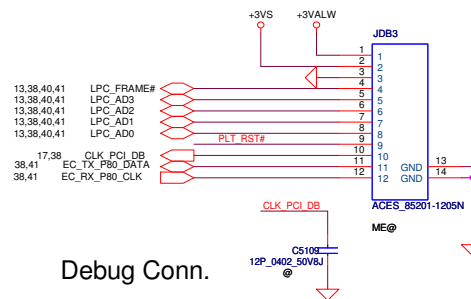
Touch Panel




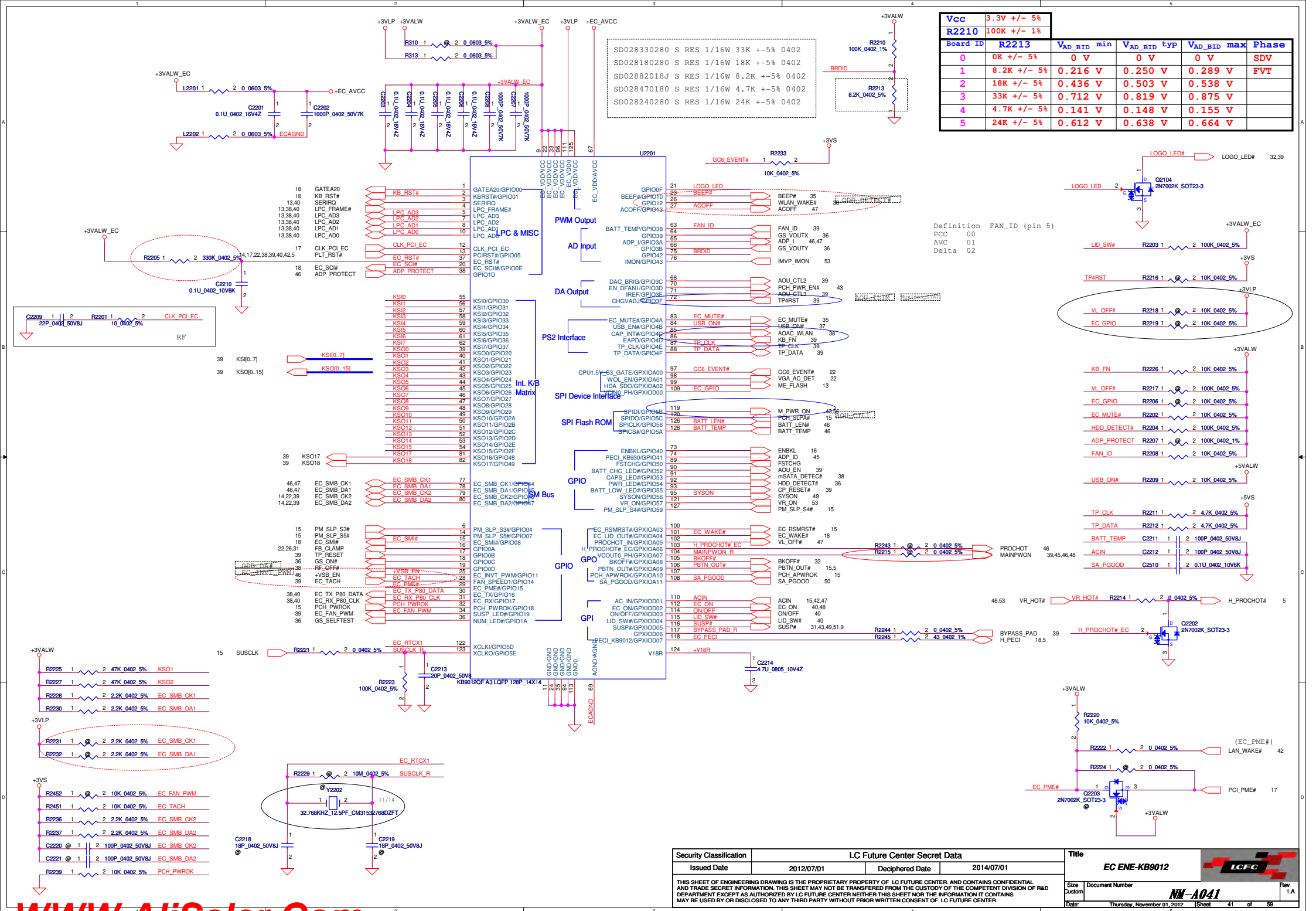
TPM

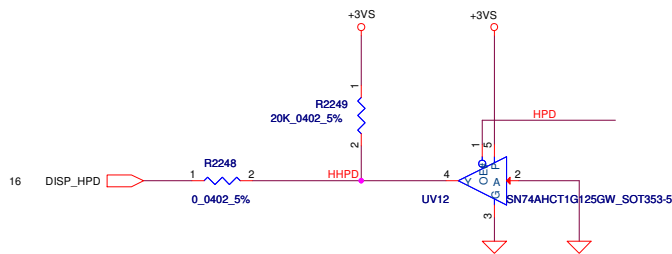


Debug Conn.

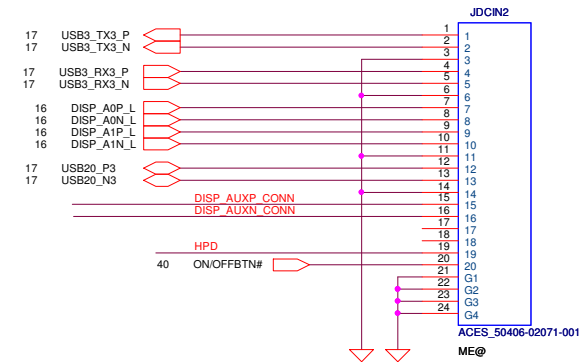
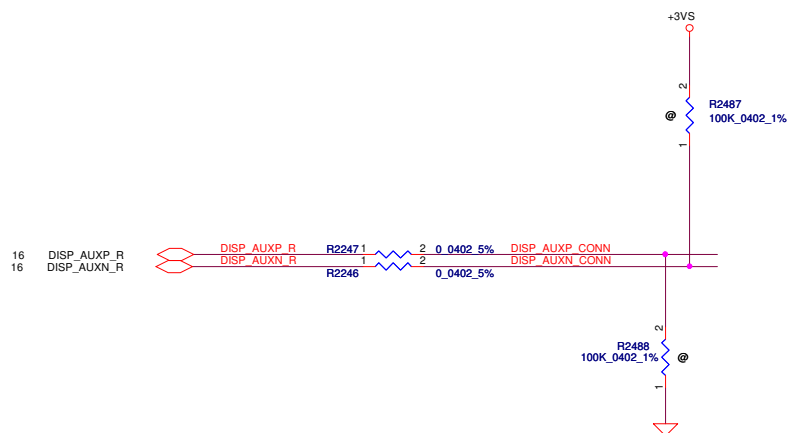


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				Date:	Wednesday, November 07, 2012	Sheet 40 of 59 Rev 1A

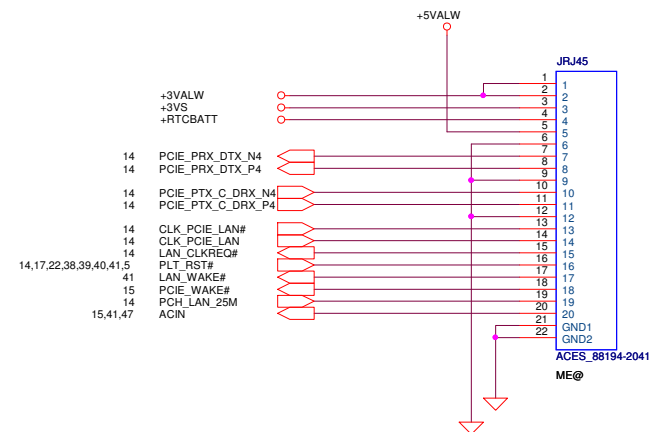





DP/TMDS Switch Circuit (1)

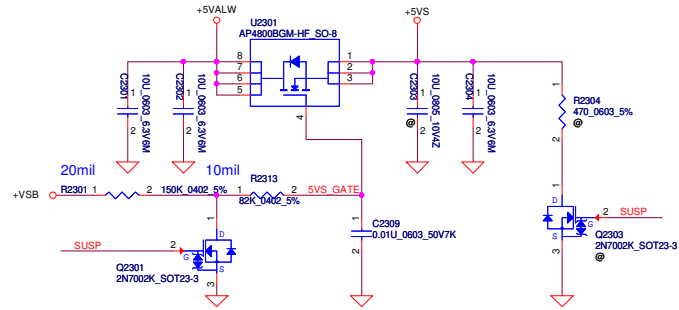


RJ45 Board

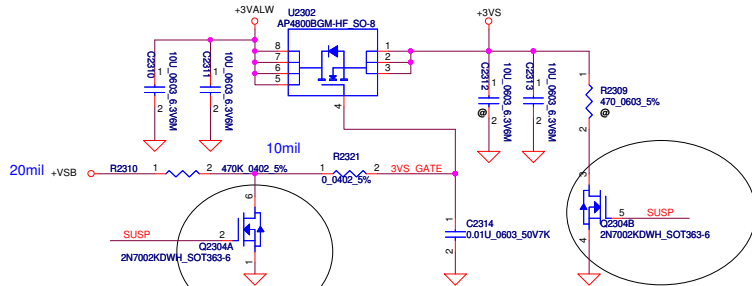


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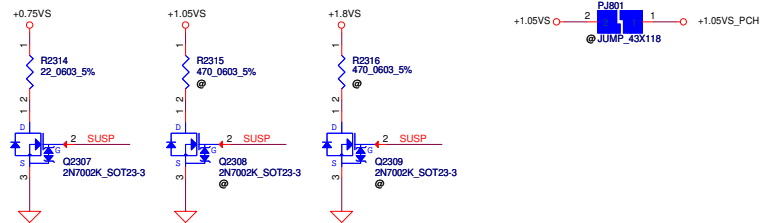
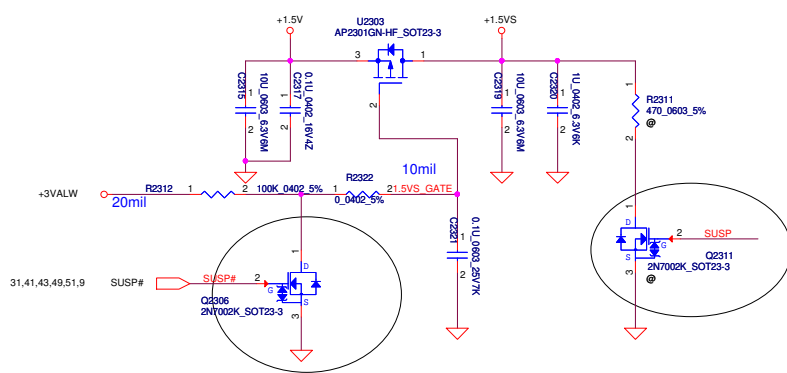
+5VALW TO +5VS



+3VALW TO +3VS

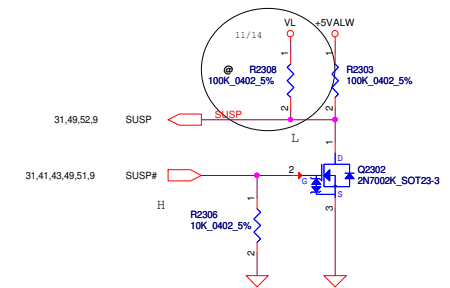
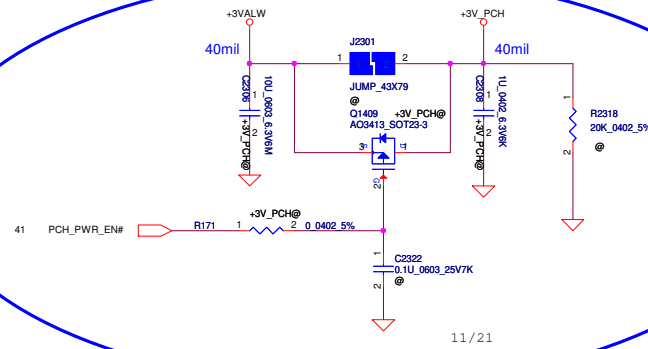


+1.5V to +1.5VS

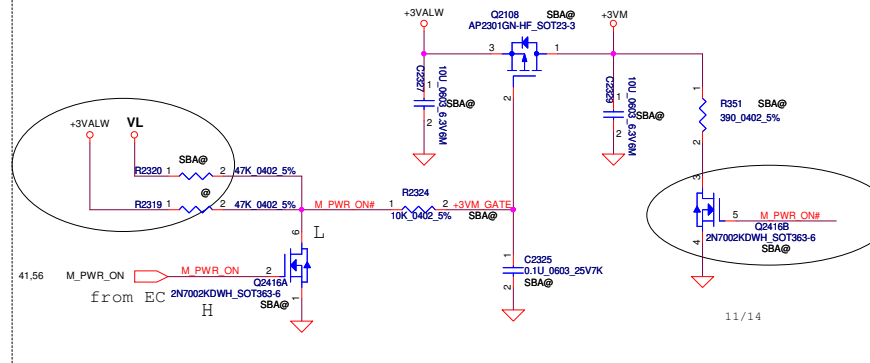


+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3

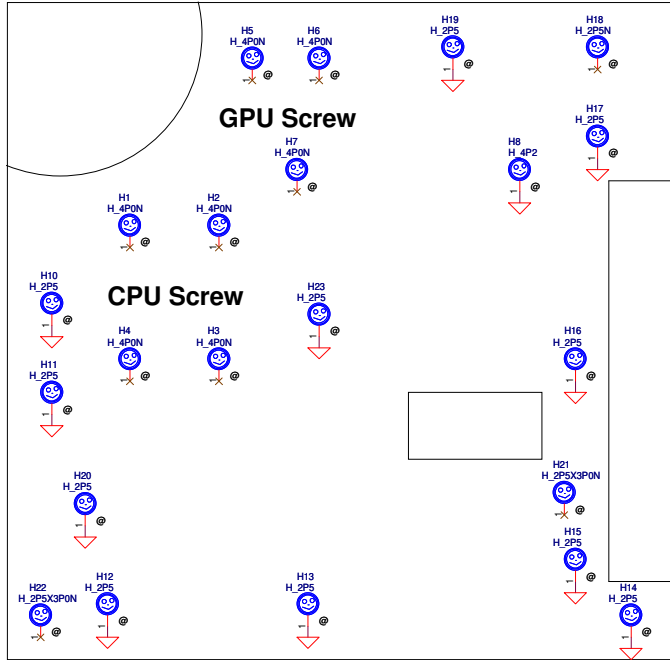


FOR SBA Function POWER(always mount)

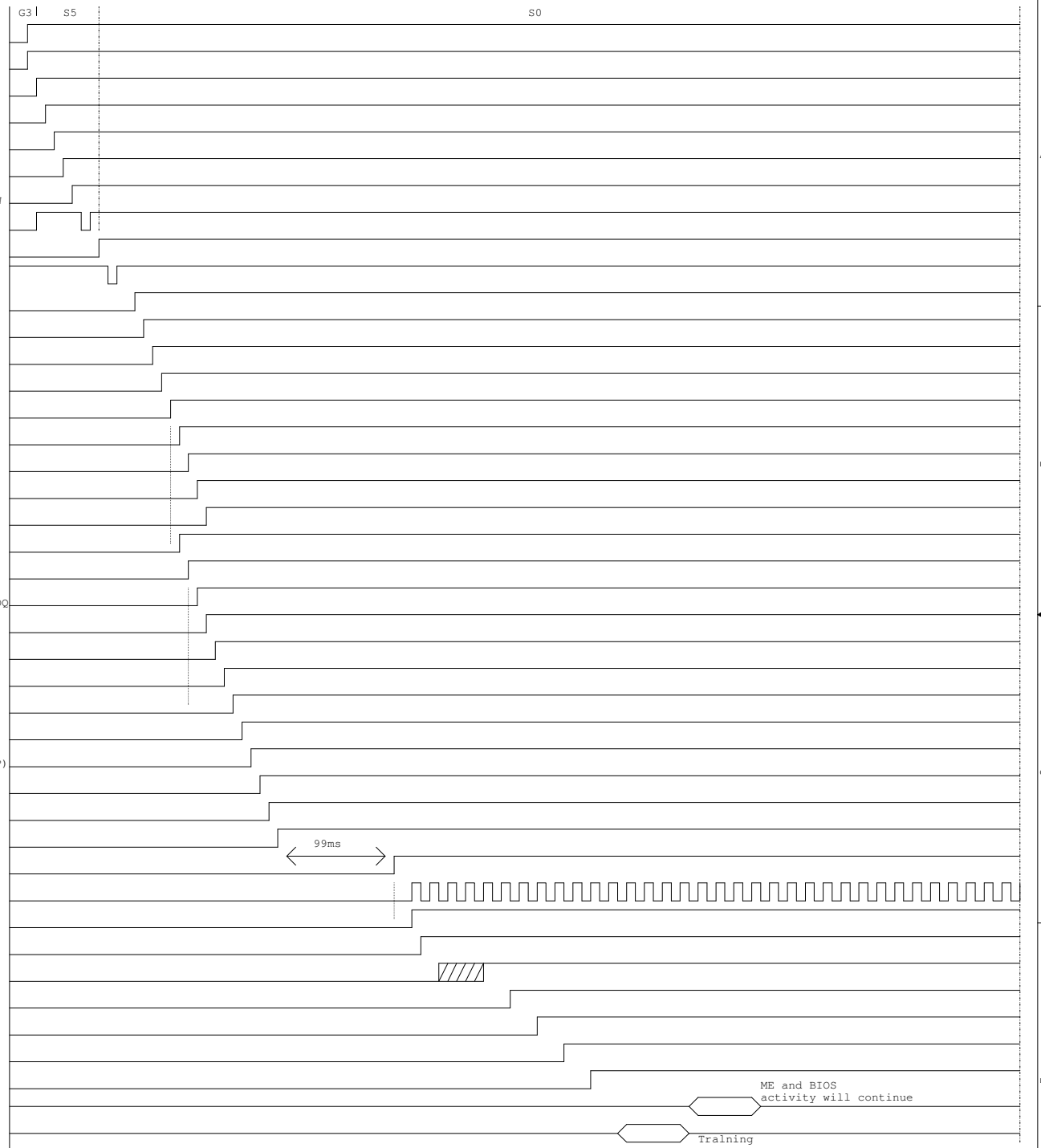


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Screw Hole & FD



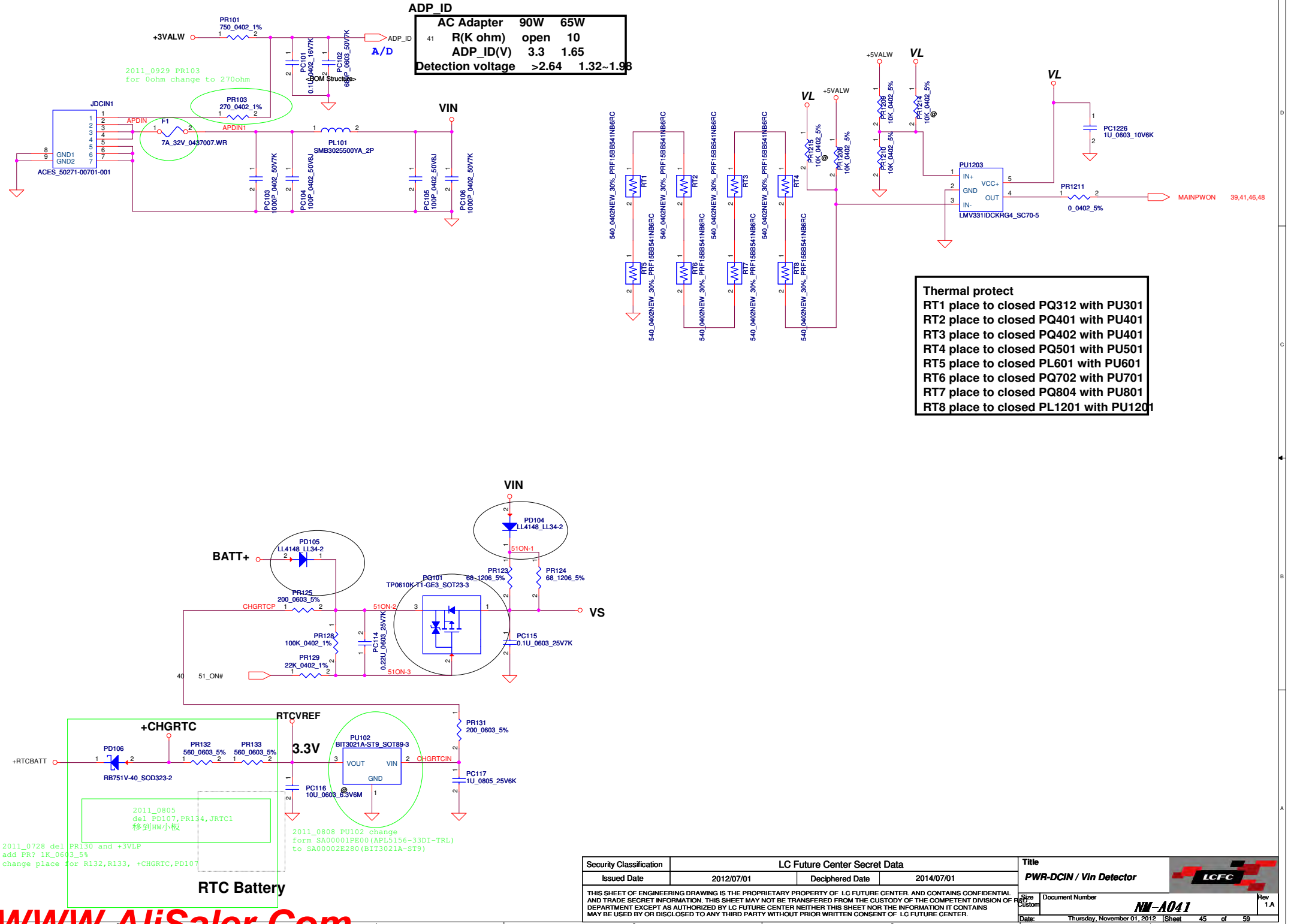
RTC
RTCRST
EC_111 pin
EC_ON
MAINPWON
+5VALW
+3VALW/VCCDSW
ON/OFF#
EC_RSMRST#
PBTN_OUT#
SLP_S5#
SLP_S4#
SYSON
SYSON
PCH_SLPA#
M_PWR_ON
+3VM
+1.05VM
PCH_APWROK
SLP_S3#
SUSP#
+1.5V_CPU_VDDQ
+1.8VS
+5VS
+3VS
+1.5VS
+0.75VS
+V1.05VS (VCCP)
+VCCSA
SA_PGOOD
VR_ON
PCH_POK
PCH_CLKOUT
DRAMPWROK
H_CPUPWRGD
CPU_VID
CPU_CORE
VGATE
SYS_PWROK
BUF_PLT_RST#
SPI
DMI



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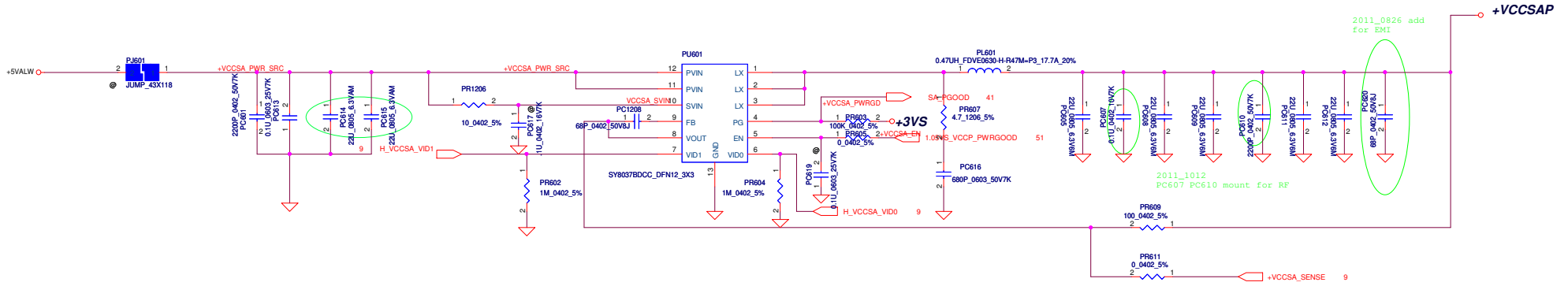
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

```
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
```

+VCCSAP 2 PJ602 1 **+VCCSA**
 @ JUMP_43X118

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

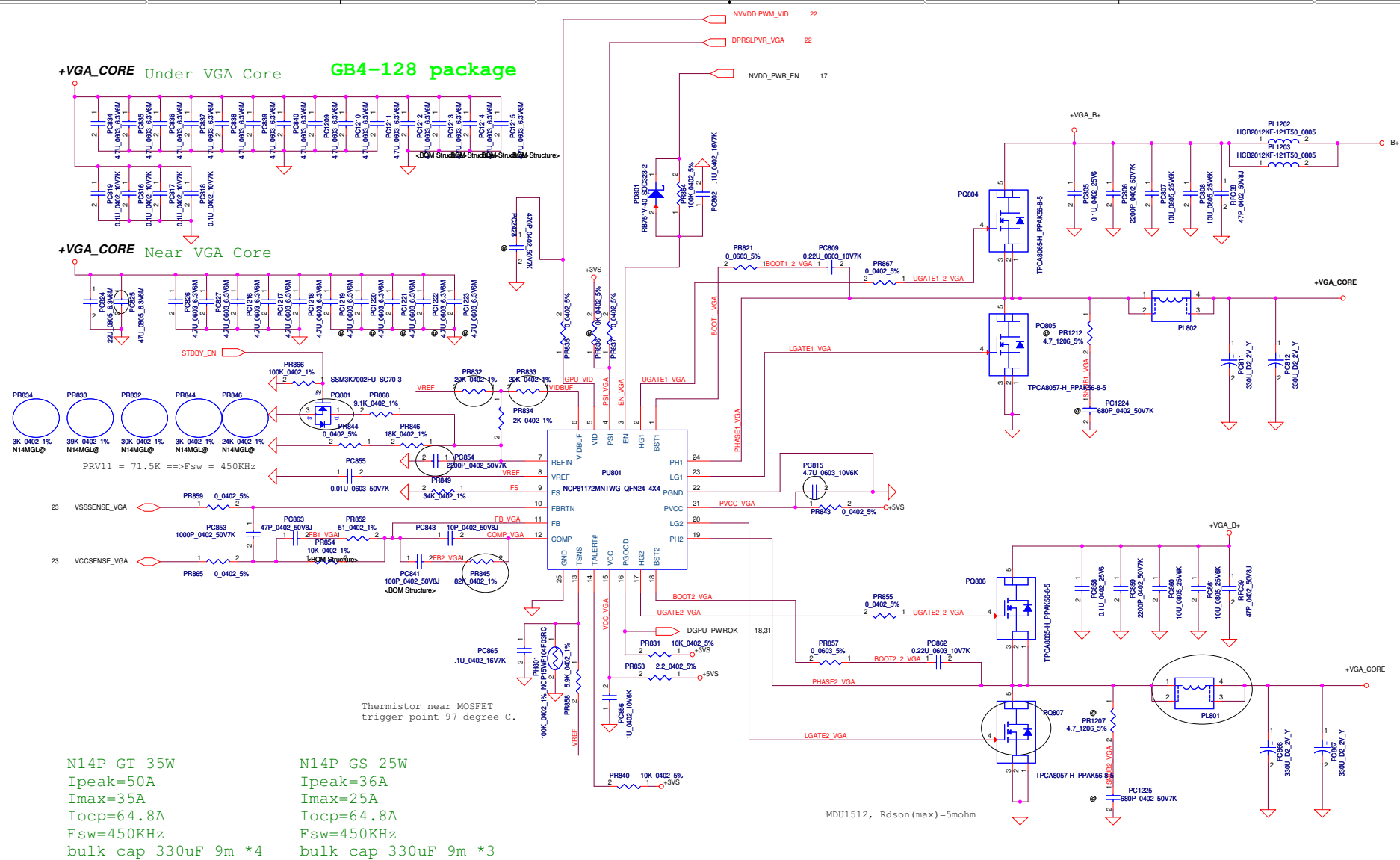


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Title	<i>PWR-VCCSAP</i>
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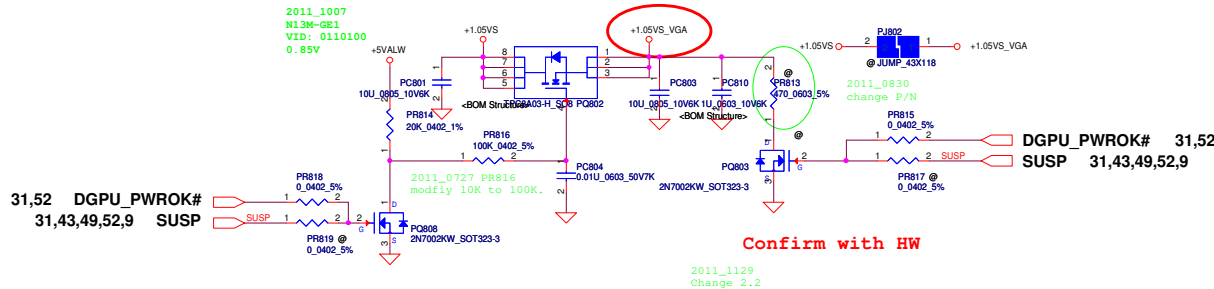
Size	Document Number	Rev
C	NM-A041	1.A




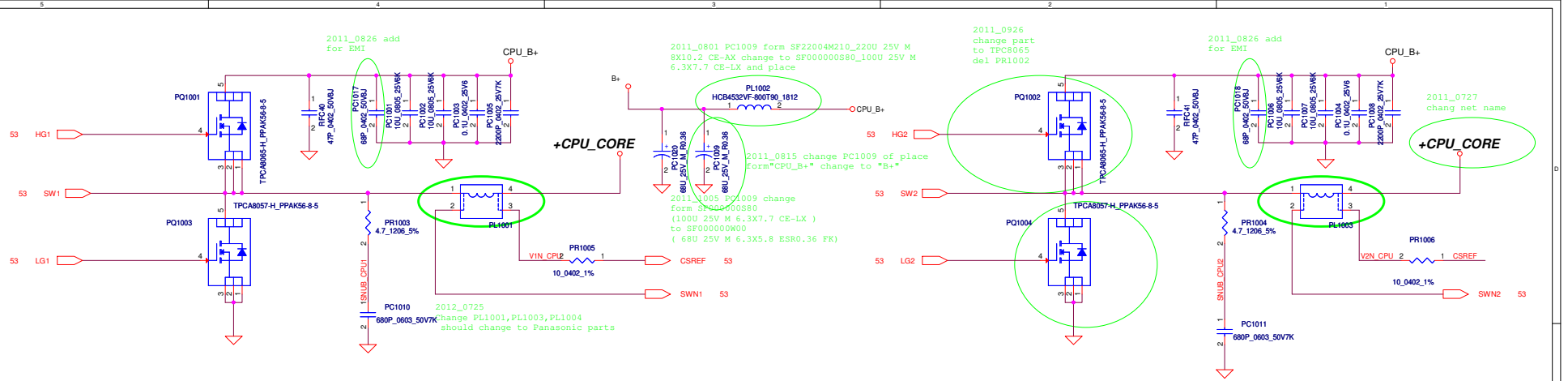
N14P-GT 35W
Ipeak=50A
Imax=35A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *4

N14P-GS 25W
Ipeak=36A
Imax=25A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *3

MDU1512, Rsdn (max)=5mohm

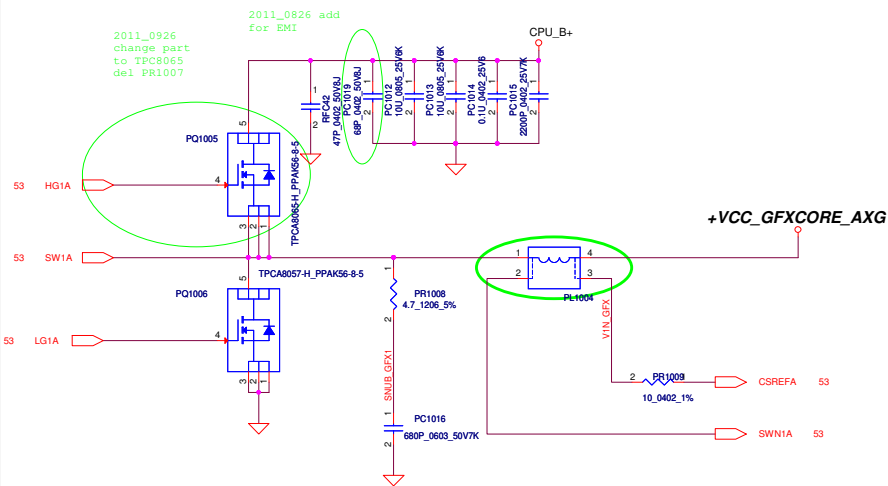


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2012/07/01		2014/07/01			
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QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP-110A

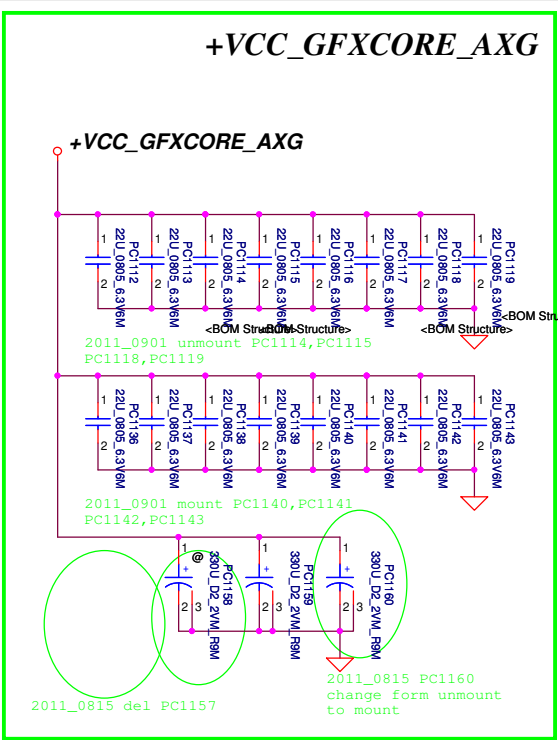
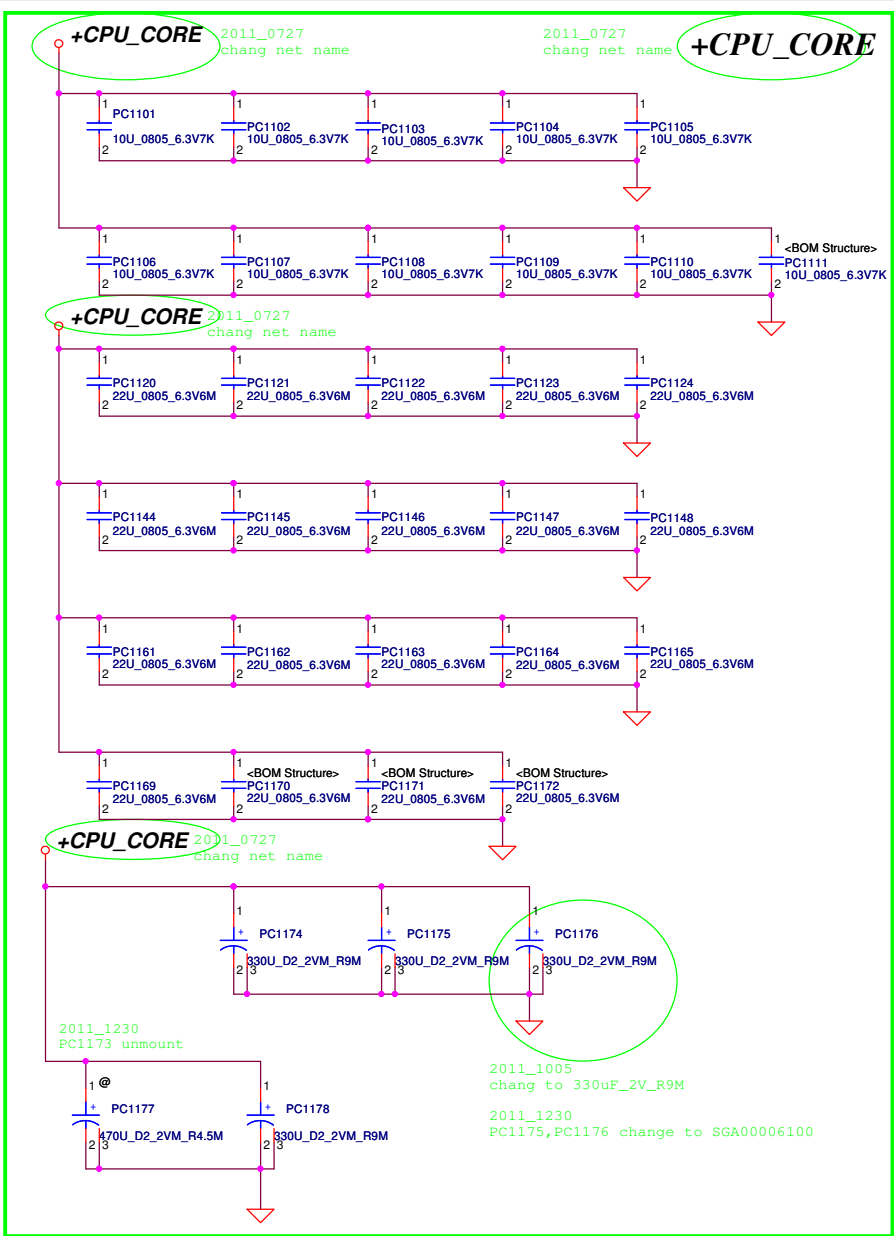
DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP-65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

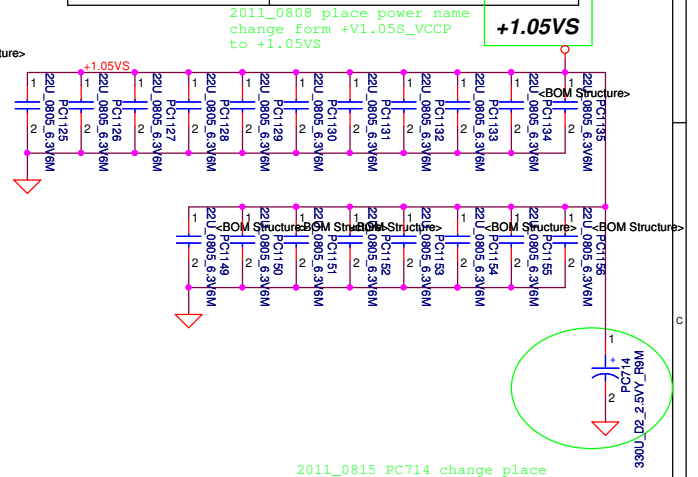
DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

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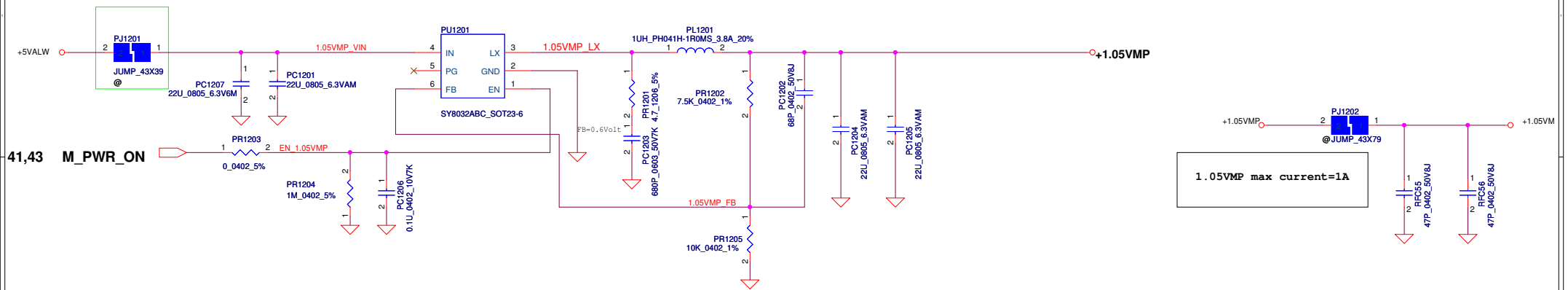


Below is 458544_CRV_PDDG_0.5 Table 5-8.

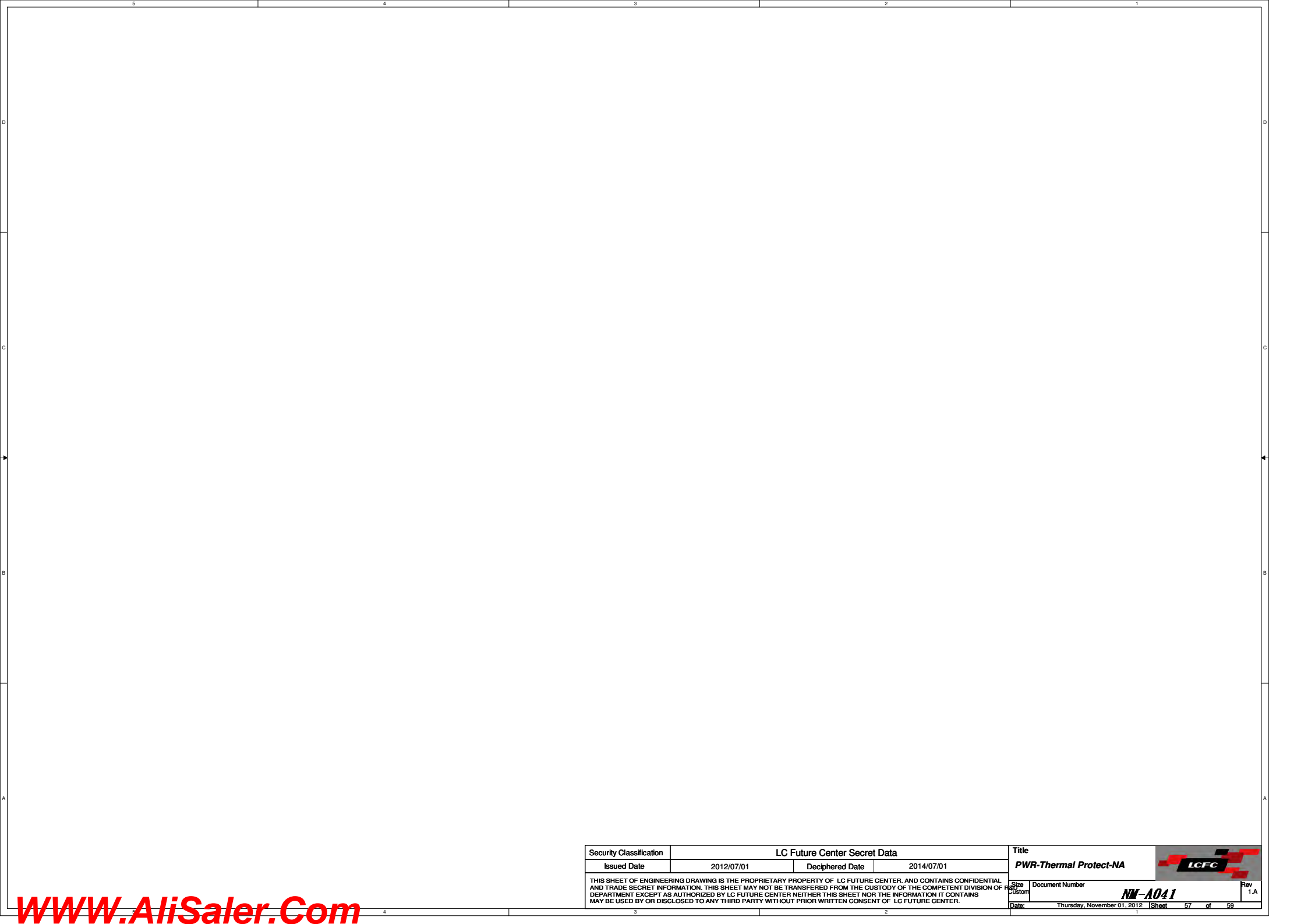
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites




2011_0923 JUMP form 43X79 change to 43X79



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				Date: Thursday, November 01, 2012	Sheet 57	Rev 1.A

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2012/09/XX	No1	V	V	V	Add CXXX, CXXX	Add XXX function

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Issued Date		Deciphered Date		EE P.I.R.	
2012/07/01		2014/07/01			
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<small>Date:</small> Thursday, November 01, 2012				<small>Rev</small> 1.A	
<small>Sheet</small> 59 <small>of</small> 59					